NXP's Mini Logic portfolio

When first introduced, logic product offerings consisted of quad, hex and octal standard logic gates, inverters and buffers. Entire applications were built from these building blocks. As integration and miniaturization occurred, the demand for logic solutions continued to grow, but shifted toward "control" or "glue" logic. Control logic allows seamless connections between highly integrated circuits and enables designers to add capabilities not yet integrated into the system controller. It supports last minute feature additions, and enables minor design corrections, thereby reducing the effect of any design changes on time-to-market.

With the shift to control logic, engineers left much of the standard logic solution unused, often only using one or two of the four logic gates in a quad device. However, this situation posed a problem when circuit boards became increasingly complex and more densely packed, necessitating logic and voltage translation solutions tuned to the exact electrical and physical specifications of the application, and with no margin for inefficient use of components. The larger pin count and package sizes available in standard logic also complicated layout and hindered smaller form fit applications.

As the leading innovator in package technology, NXP introduced Mini Logic to address these issues. It provides logic solutions in single-, dual-, and triple-gate leaded (PicoGate) and leadless (MicroPak) packages, simplifying layout and reducing footprint by 85% or more. Designers can now combine the logic function and package footprint that best suits the application.

NXP's Mini Logic portfolio streamlines board design

NXP offers the largest, most comprehensive portfolio of 0.8 V to 5.0 V Mini Logic products, and invented the 5-pin MicroPak package—the world's smallest 5-pin logic package. In 2013, NXP also released the AXP family of Mini Logic solutions, which offers the lowest power logic solutions—another Mini Logic innovation enabling smaller form factors through reduced battery sizes for equivalent operational duration.

Whether an application requires low voltage, low power, or the stringent requirements of automotive qualification, NXP has the ideal Mini Logic solution to help.

NXP's Mini Logic portfolio comprises single-, dual-, and triple-gate functions in small 5-, 6-, 8- or 10-pin packages. Logic families that have been released in Mini Logic include AXP, AUP, AHC(T), AVC, CBT, CBTLV, HC(T) and LVC. Table 1 illustrates the features of these families. As opposed to traditional quad-gate solutions, Mini Logic allows designers to select the specific number of functions required. This greater efficiency enables more intricate line layout patterns, while saving up to 85% of board space.

Table 1. Mini Logic families

High voltage family	HC(T)	AHC(T) / XC7	CBT(D)
Supply voltage	2 to 6 V	2 to 5.5 V	4.5 to 5.5 V
Typ. prop delay	9 ns	5 ns	0.25 ns
Output drive	± 8 mA	± 8 mA	N/A
Standby current	80 µA	40 µA	3 µA
Tamb	-40 °C to 125 °C	-40 °C to 125 °C	-40 °C to 85 °C
AEC-Q100 option	•	•	•
Features	Input clamp diodes, TTL input option	5 V tolerant inputs, TTL input option	Low density isolation

Low voltage family	AVC(M)	LVC	AUP	AXP
Supply voltage	1.2 to 3.6 V	1.65 to 5.5 V	0.8 to 3.6 V	0.7 to 2.75 V
Typ. prop delay	2 ns	2 ns	4 ns	3 ns
Output drive	± 8 mA	± 24 mA	± 4 mA	± 8 mA
Standby current	20 µA	20 µA	0.9 µA	0.6 µA
Tamb	-40 °C to 85 °C	-40 °C to 125 °C	-40 °C to 125 °C	-40 °C to 85 °C
AEC-Q100 option	•	•	•	
Features	3.6 V tolerant inputs, Bus hold and series dampening resistor options, Power off disable	5 V tolerant inputs, Bus hold and series dampening resistor options, Power off disable	3 V tolerant inputs, Low threshold input options, Power off disable	3 V tolerant inputs, Power off disable

The Mini Logic packages house the same logic families as the larger SO, TSSOP & DQFN packages. Whereas the 74LVC08 is a quad 2-input AND gate, the 74LVC1G08 Mini Logic device is a single 2-input AND gate. These packages allow the use of single gates rather than using one gate of a quad or hex device. Figure 1 shows the effect of replacing a quad 2-input AND gate, in which only one device is used, with a Mini Logic single 2-input AND gate. Many applications can benefit from the form factor reduction Mini Logic provides. The use of Mini Logic and the reduction in printed circuit board area also results in significant system level cost reduction.

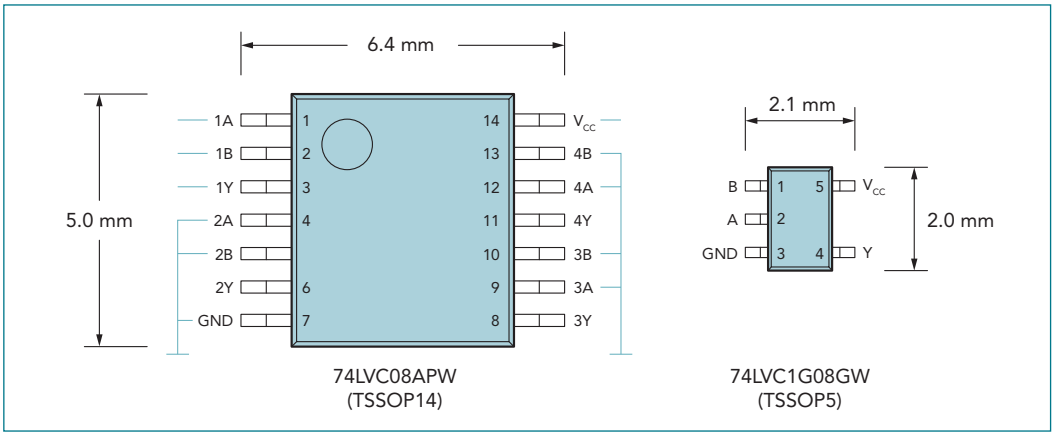


Figure 1. Comparison of 74LVC08APW vs 74LVC1G08GW PCB footprints

In addition to reducing the complexity of board layout, Mini Logic devices are a highly efficient means of implementing glue logic to support last minute feature additions and improve time-to-market. Their small size and lower power consumption makes them especially suited for portable electronic devices.

Leaded Mini Logic packages are known as PicoGates, and are available with 0.95 mm, 0.65 mm, and 0.5 mm pin pitch. Leadless Mini Logic packages are known as MicroPak, and are available with 0.5 mm, 0.35 mm, and 0.30 mm pad pitch.

PicoGate family of leaded package Mini Logic

The PicoGate packages include the 8-pin VSSOP (SOT765-1), 10-, 8-, 6-, and 5-pin TSSOP (SOT552, SOT505-2, SOT363, and SOT353) as well as 6- and 5-pin TSOP (SOT457 and SOT753). See Table 1 for a summary of package dimensions.

Logic families released in Mini Logic PicoGate include AUP, AHC(T), AVC, CBT, CBTLV, HC(T), and LVC. These products are all Pb-free, RoHS and dark green compliant, and designed for use in ambient temperatures between -40°C and 125°C. The Mini Logic PicoGate range of products includes Q100 variants that meet the AEC-Q100, grade 1 standard, and are suitable for automotive applications. PicoGate pin pitches include 0.95 mm, 0.65 mm, and 0.5 mm.

Table 2. Mini Logic PicoGate package range

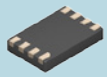
Package suffix	GW	GV	GW	GV	DP	DC	DP
	TSSOP5	TSOP5	TSSOP6	TSOP6	TSSOP8	VSSOP8	TSSOP10
							
Package	SOT353-1	SOT753	SOT363	SOT457	SOT505-2	SOT765-1	SOT552
Width (mm)	2.10	2.75	2.10	2.75	4.00	3.10	4.90
Length (mm)	2.00	2.90	2.00	2.90	3.00	2.00	3.00
Height (mm)	1.00	1.00	1.00	1.00	1.10	1.00	1.10
Pitch (mm)	0.65	0.95	0.65	0.95	0.65	0.50	0.65

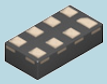
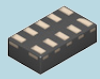
MicroPak family of leadless package Mini Logic

The MicroPak packages include the 10- and 8-pin XQFN (SOT1160 and SOT902), 10-, 8-, and 6-pin XSON (SOT1081, SOT996, SOT833, SOT1089, SOT1116, SOT1203, SOT886, SOT891, SOT1115 and SOT1202) as well as 5-pin X2SON (SOT1226). See Table 3 for a summary of package dimensions.

Logic families released in Mini Logic MicroPak include AXP, AUP, AHC(T), AVC, CBT, CBTLV, HC(T), and LVC. Like the PicoGate family, these products are all Pb-free, RoHS, and dark green compliant, and designed for use in ambient temperatures between -40°C and 125°C. The Mini Logic MicroPak range of products includes Q100 variants that meet the AEC-Q100, grade 1, and are suitable for automotive applications. MicroPak pin pitches include 0.5 mm, 0.35 mm, and 0.3 mm.

Table 3. Mini Logic MicroPak package range

Package suffix	GX	GM	GF	GS	GN	GD	GM
	XSON5	XSON6	XSON6	XSON6	XSON6	XSON8	XQFN8
							
Package	SOT1226	SOT886	SOT891	SOT1202	SOT1115	SOT996-2	SOT902-2
Width (mm)	0.80	1.00	1.00	1.00	1.00	3.00	1.60
Length (mm)	0.80	1.45	1.00	1.00	0.90	2.00	1.60
Height (mm)	0.35	0.50	0.50	0.35	0.35	0.50	0.50
Pitch (mm)	0.50	0.50	0.35	0.35	0.30	0.50	0.50

Package suffix	GT	GF	GS	GN	GU	GF
	XSON8	XSON8	XSON8	XSON8	XQFN10	XSON10
						
Package	SOT883-1	SOT1089	SOT1203	SOT1116	SOT1160-1	SOT1081-2
Width (mm)	1.00	1.00	1.00	1.00	1.40	1.00
Length (mm)	1.95	1.35	1.35	1.20	1.80	1.70
Height (mm)	0.50	0.50	0.35	0.35	0.50	0.50
Pitch (mm)	0.50	0.35	0.35	0.30	0.40	0.35

Innovation in Mini Logic

NXP is a true innovator in logic products. The advanced ultra-low power (AUP) and advanced extremely low power (AXP) logic families are the two lowest power logic families currently available. Both families have been initially released solely in the Mini Logic portfolio.

Advanced Ultra-low Power logic (AUP)

The AUP family is the industry standard family for portable applications. NXP manufactures the AUP family in a CMOS process, resulting in lower static and dynamic power dissipation. Its 3.6 V tolerance, low-threshold inputs (option) and I_{OFF} features make it suitable for use in mixed 1.8 V / 3.3 V and partial power-down applications. The family is fully specified from 1.1 V to 3.6 V, and for industrial and automotive operating temperatures. The product portfolio is available in leaded and leadless Mini Logic packages and includes low pin count single-, dual- and triple-gate functions as well as configurable logic.

Advanced eXtremely-low Power logic (AXP)

AXP logic provides a speed upgrade to the AUP logic family. However, unlike previous high-speed solutions (AUC, ULP, and ULP-A), it does so without increasing dynamic power dissipation. Fully specified from 0.75 V to 2.75 V, AXP logic is suitable for existing 2.5 V and 1.8 V applications, while supporting the trend to the lower 1.2 V and 0.8 V voltage nodes. AXP products are available in innovative leadless Mini Logic XSON and X2SON packages for PCB space saving, and include low pin count single-, dual-, and triple-gate functions as well as configurable logic.

Power dissipation versus performance of NXP Mini Logic

At a supply voltage of 3.3 V, NXP's AUP is the lowest power logic family with the highest performance. With supply voltages of 2.5 V and lower, AXP is the lowest power logic family with the highest performance. Power dissipation of CMOS logic is linear with frequency. As a result, for first order dynamic power dissipation calculations, a CMOS logic device can be modeled as a capacitor (C_{PD}). When developing low power logic solutions, the goal is to target the lowest possible C_{PD}. Figure 2 shows a comparison of the AUP and AXP logic families with other low power solutions currently available.

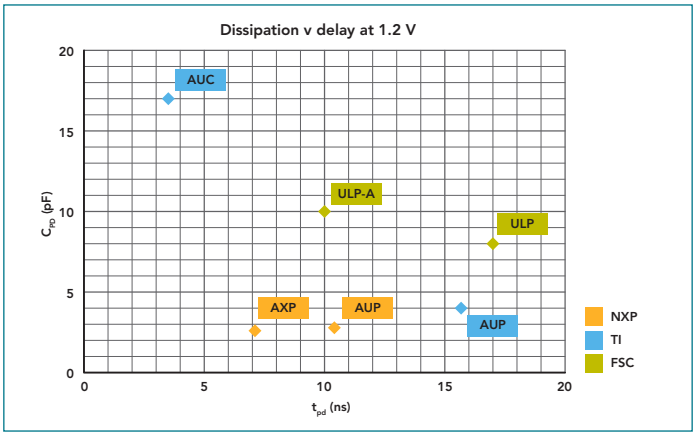


Figure 2. Dynamic power dissipation vs propagation delay for low power logic solutions

Figure 3 shows that as the supply voltage of an application decreases to the 2.5 V node or below, AXP is the lowest power family.

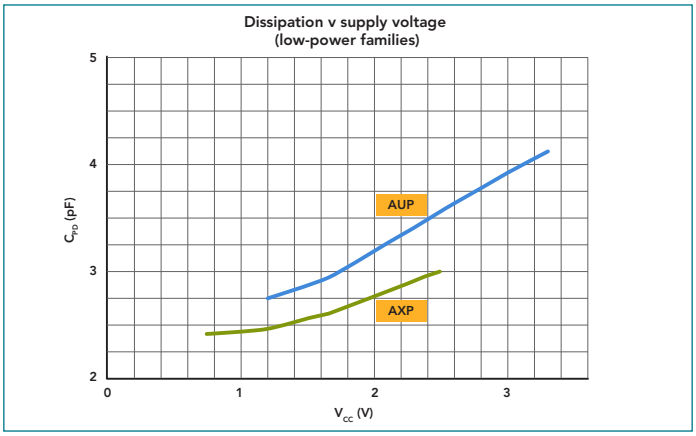


Figure 3. Dynamic power dissipation versus supply voltage for AUP and AXP Families

Configurable Logic

NXP also works with its partners to integrate more features and functionality into the Mini Logic portfolio. In this way, Mini Logic offers further space, power and cost savings. The introduction of configurable logic into the Mini Logic portfolio is just one example of the innovation taking place in the portfolio.

A configurable logic device is a single logic device that can be "configured" by the PCB layout to provide one of several different logic functions. Configurable logic is not the same as programmable, because all devices are identical and do not need to be programmed before use. The configuration of the power, ground and select pins on the device determines selection of the particular logic function. For example, the 74AUP1G57 can provide any one of the following standard functions: AND, NAND, OR, NOR, XNOR, inverter, or buffer, as well as non-standard combinations (e.g., a NAND gate with one input inverted).

NXP's configurable logic allows design flexibility, reduces inventory cost and accelerates qualification for customer applications. By combining more than one function into a single package and offering the flexibility to configure them separately, engineers always have glue logic readily available to economically solve any design issue.

Figure 4 shows the configurable logic gate 74AUP1G57 configured as the non-standard function 2-input OR gate with one input inverted. Because configurable logic products include Schmitt-trigger inputs as standard, to generate this non-standard function using existing gates would require functions 1G14, 1G17, and 1G32 combined as shown in Figure 5. The integration of functionality into a single Mini Logic device represents savings in power consumption, board space and system cost.

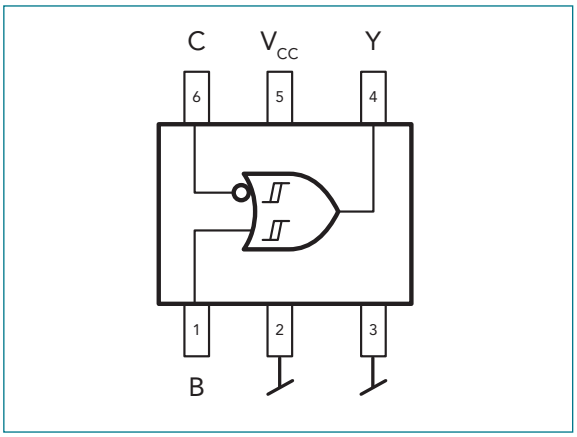


Figure 4. 74AUP1G57 configured as a 2-input OR Gate with one input inverted

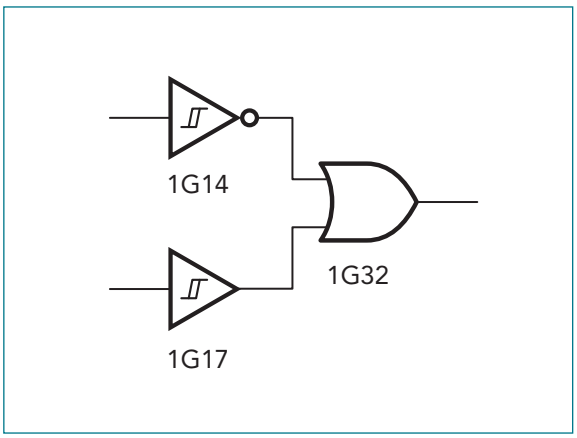


Figure 5. 2-input OR Gate with one input inverted and Schmitt-trigger made from discrete logic

Package Quality Assurance

To ensure product quality and reliability, NXP subjects the Mini Logic packages to multiple stress and accelerated life tests before release, and at regular intervals thereafter. NXP publishes results of its ongoing reliability-monitoring program quarterly. The following paragraphs describe the stress tests.

PCON – Preconditioning (Q100 code 'PC' reference JESD22 A113 J-STD-020)
Prior to a number of qualification stress tests, the SMD devices undergo preconditioning, which NXP performs in line with the latest revision of the IPC/JEDEC Standard J-STD-020C (as described in NXP Semiconductors specification SNW-FQ-225A). The expected outcome is that these packages will have a moisture sensitivity level (MSL) of "1," indicating that the products are not sensitive to moisture.

The following steps summarize the preconditioning sequence:

- Moisture soak for 168 hours at 85 °C/85% R.H.
- Within four hours, exposure three times to IR soldering. (Temperature 260 °C +5/-0)
- Flux, rinse, and dry
- Electrical test

EFR—Early Failure Rate (Q100 code 'ELFR' reference AEC-Q100-008)
(Electrical endurance with electrical bias (V_{CC}, max x 1.2) at 150 °C)
The early failure rate test is the primary test for determining the short-term reliability of the product, as well as determining gate oxide, metallization layer and other infant mortality defects. Burn-in requirements depend upon the product maturity and the supplier's ability to demonstrate that known defect mechanisms have either been eliminated, or that adequate test screens are in place to capture intrinsic and random defects.

HTOL / SHTL—Static High Temperature Life (Q100 code 'HTOL' reference JESD22 A108)
(Electrical endurance with electrical bias (V_{CC}, max x 1.2) at 150 °C)
The static high temperature life test is the primary test for determining the long-term reliability of the product. Generally, the package has limited influence on this test. It is nevertheless included to demonstrate the long-term reliability of the product/package combination.

HAST / THB—Highly Accelerated Steam Test (Q100 code 'THB / HAST' reference JESD22 A101 / JESD22 A110) (130 °C/85% R.H., with electrical bias (V_{CC}, max) and preconditioning)
The highly accelerated steam test stresses both the electrical endurance of the design/process, as well as the resistance to moisture of the package.

TMCL / TC—Temperature Cycling (Q100 code 'TC' reference JESD22 A104)
(Air to air -65 °C +150 °C with preconditioning)
The temperature cycling test aims to ensure the mechanical integrity of the whole product, under several circumstances of rapid changes in temperature.

HTSL—High Temperature (150°C) Storage of Devices (Q100 code 'HTSL' reference JESD22 A103)
The high temperature storage test evaluates the reliability of the product after long-term storage.

PPOT / UHAST / AC—Unbiased Pressure Pot Test (Q100 code 'AC / UHST' reference JESD22 A102 / JESD22 A118) (Autoclave (121 °C, 100% R.H.), with preconditioning)
The unbiased pressure pot test test evaluates the moisture resistance of the package.

Summary

Due to integration of functionality, a need arose for control logic in many complex and densely packed circuit boards. NXP introduced Mini Logic to address this need, and now has the largest portfolio in both leaded (PicoGate) and leadless (MicroPak) packages to support this smaller footprint application trend. To ensure trouble free product operation over the lifetime of an application, NXP subjects the Mini Logic portfolio to rigorous qualification stresses and ongoing reliability monitoring.

With continuous innovation to integrate non-standard functions and features into its lower power AUP and AXP Mini Logic portfolio, NXP continues to lead the way in reducing the power consumption, footprint and system level cost of today's applications.

For more information and to learn more about NXP Mini Logic portfolio please visit:
http://www.nxp.com/products/logic/family/MINI_LOGIC/

www.nxp.com

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