Single Pair Ethernet
10BASE-T1S

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Agenda

- **Evolution of networks**
  - Disadvantages of using multiple network technologies
  - Networks tomorrow: All Ethernet / IP architectures
- **10BASE-T1S**
  - Introduction
  - PLCA basics
- **HW implementation**
  - Bus interface network
- **Advanced features**
  - Wake and sleep
  - Credit Based traffic Shaping: CBS
  - Signal Quality Indication: SQI

Evolution of Networks

Networks and Trends Today

Disadvantages of Using Multiple Network Technologies

- **Complex architectures**
  - Almost each functional domain has its own technology
- **Expensive gateways needed**
  - to translate between different technologies
- **Each network technology has**
  - Different HW and cables
  - Different protocols and SW stacks
  - Different development tools
  - Different standards
  - Different experts

How to overcome all these disadvantages?

Migration to All Ethernet/IP Architectures

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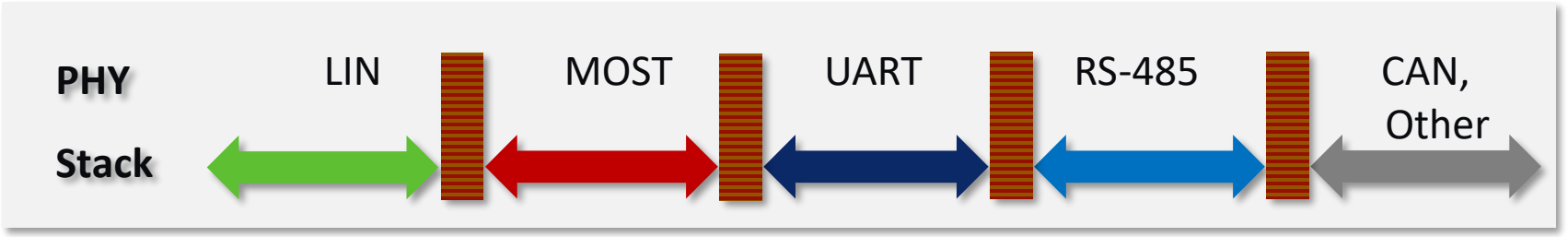
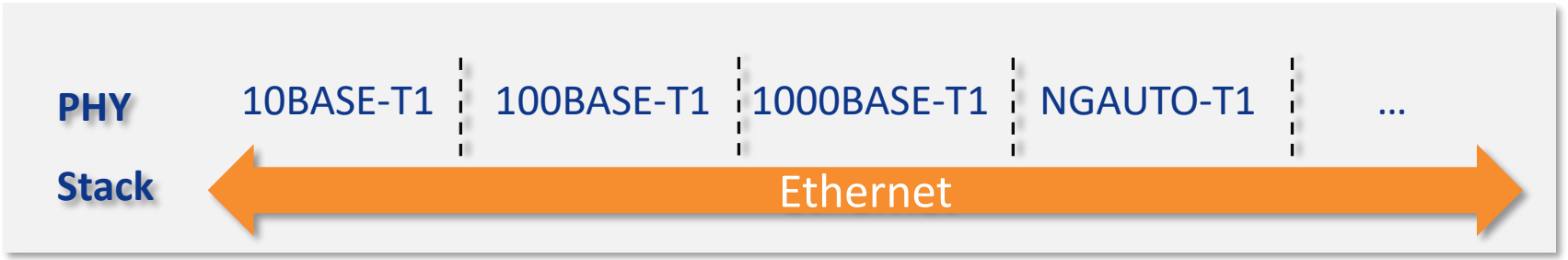
Networks Tomorrow

Advantages of All-Ethernet

Legacy network architectures



All-Ethernet/IP



- Common network software stack
- Independent of physical layer
- No gateways

Easily scalable

Many physical layers

Large ecosystem

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Networks Tomorrow

Single Pair Ethernet (SPE) – Several Speeds, Same Software

Layer 2-7 unchanged

Ethernet PHY

SPE = ‘T1’
1 balanced pair of wires

OSI Reference Model
Application
Presentation
Session
Transport
Network
Data Link
Physical Layer

Single Pair Ethernet reduces

- System cost
- Weight
- Wiring complexity

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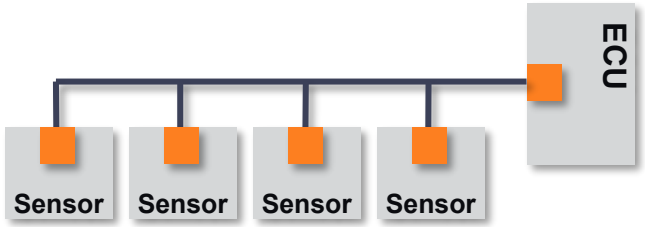
10BASE-T1S

Introduction

What is 10BASE-T1S (Short Reach)?

- **Ethernet over UTP bus**
- **10 Mbps shared**

- **Half duplex multidrop bus line**
- **Up to at least 8 nodes**
- **Up to at least 25m bus length**

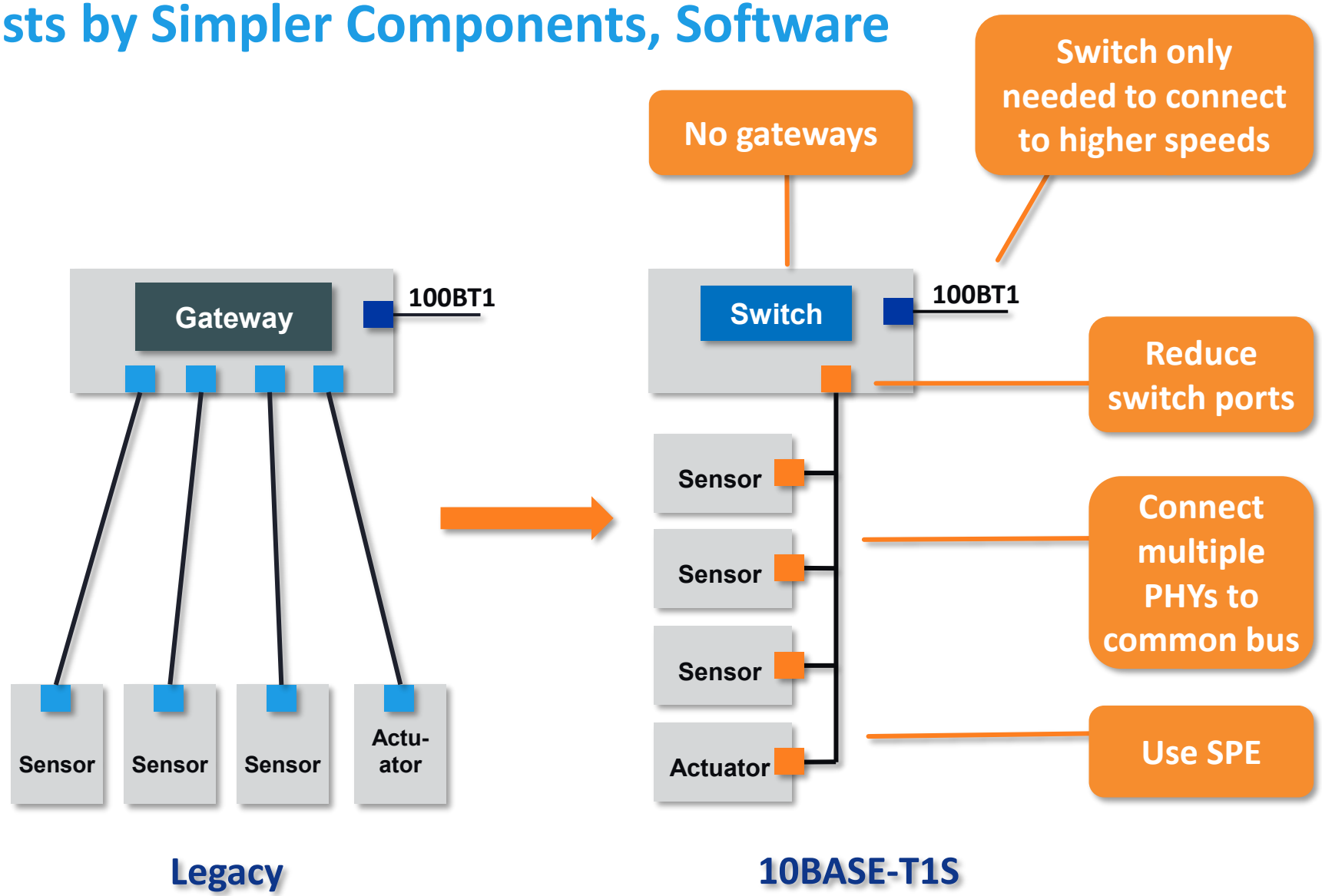


- **Half/full duplex P2P**
- **15m length**

- **IEEE 802.3cg**
- **Low power**
- **No collisions on the bus**
- **Support for**
  - AEC-Q100
  - Functional safety
  - Security
  - Time-Sensitive Networking

Benefits of 10BASE-T1S

Reduced Costs by Simpler Components, Software and Wiring



Media Access in Modern Networks: 10BASE-T1S

Carrier Sense Multiple Access / Collision Detection (CSMA/CD)

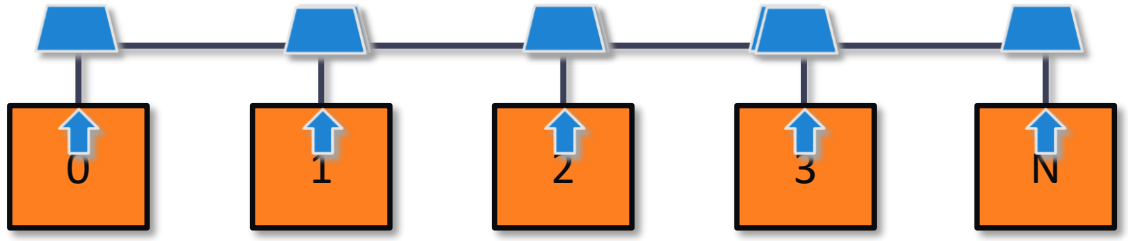
- CSMA/CD fallback supported in 10BASE-T1S

A better media access is needed:

- Full bandwidth / No collisions
- QoS / Latency calculable

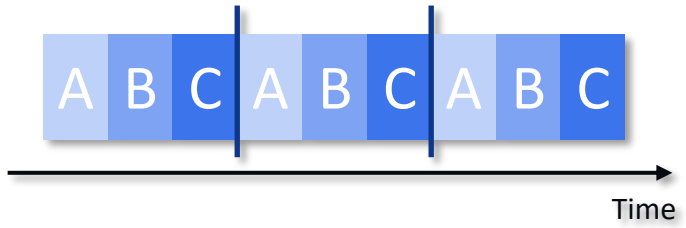
Physical Layer Collision Avoidance (PLCA)

- Shared bandwidth
- No collisions occur
- Full bandwidth available
- Latency is calculable



Application Controlled Media Access (ACMA)

- Alternative to PLCA or CSMA/CD
- Node can only send when app asserts ACMA-signal
- Collision-free time division media access



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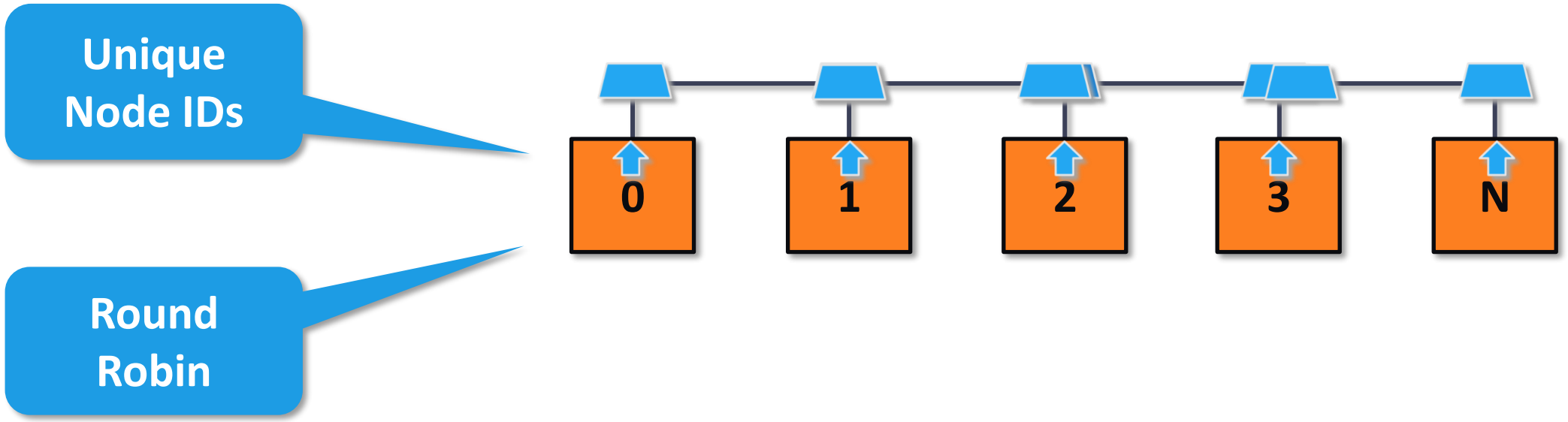
10BASE-T1S

PLCA Basics

PLCA - Basics

- Organize media access to avoid collisions
- IEEE 802.3cg - Physical Layer Collision Avoidance (PLCA)
- Each node waits for its own transmit opportunity when sending data



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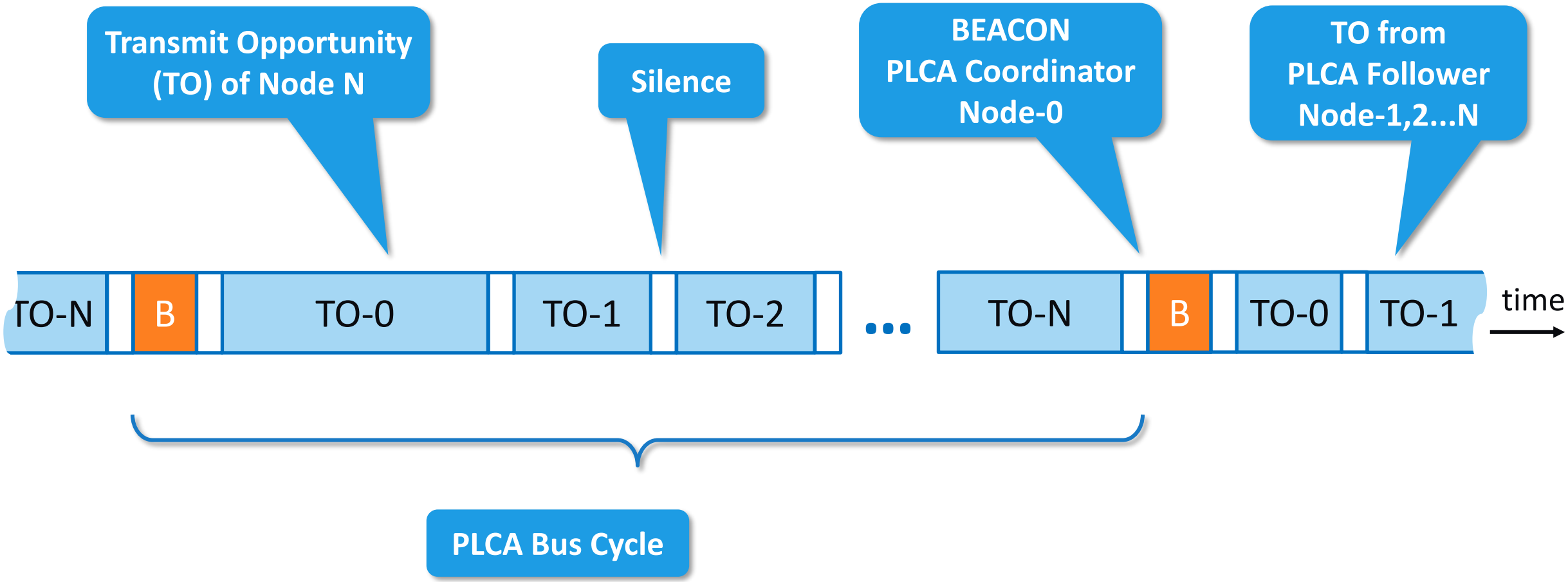
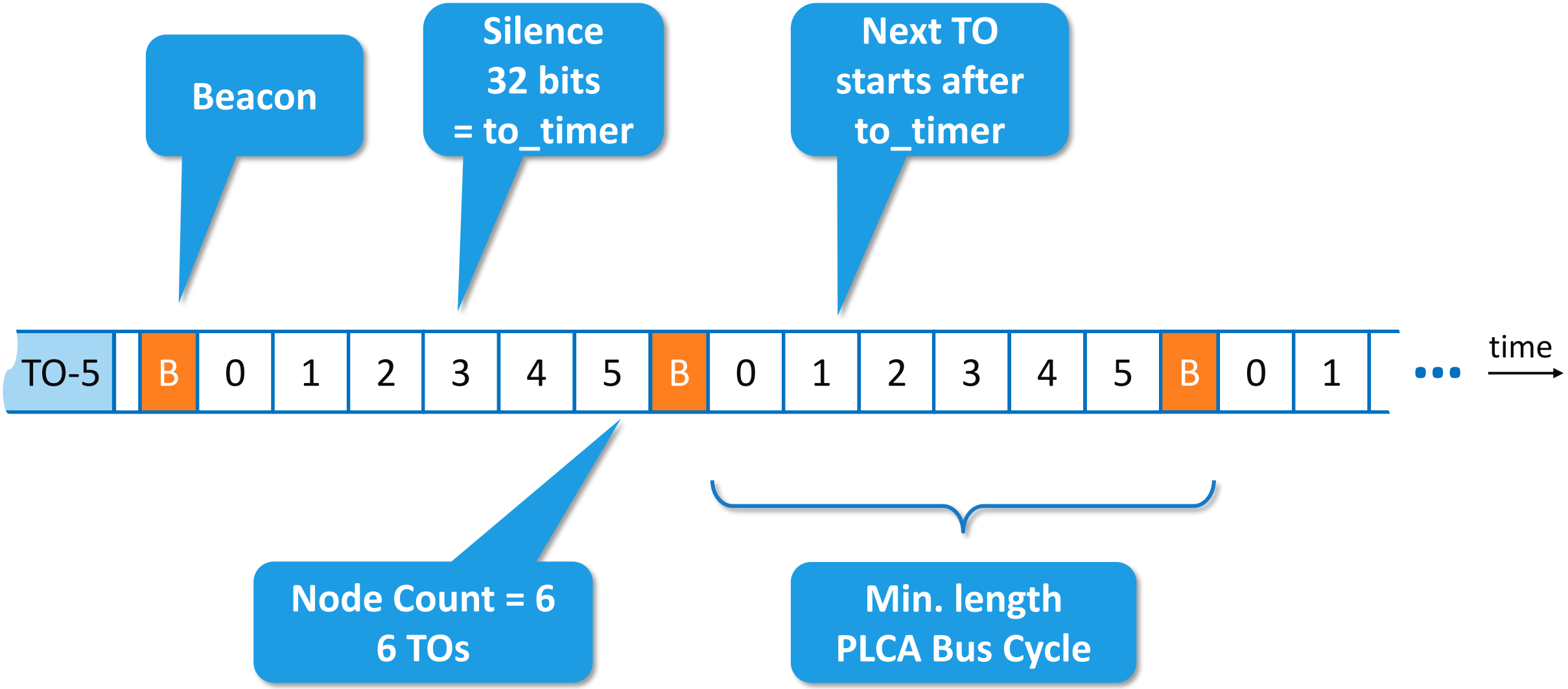
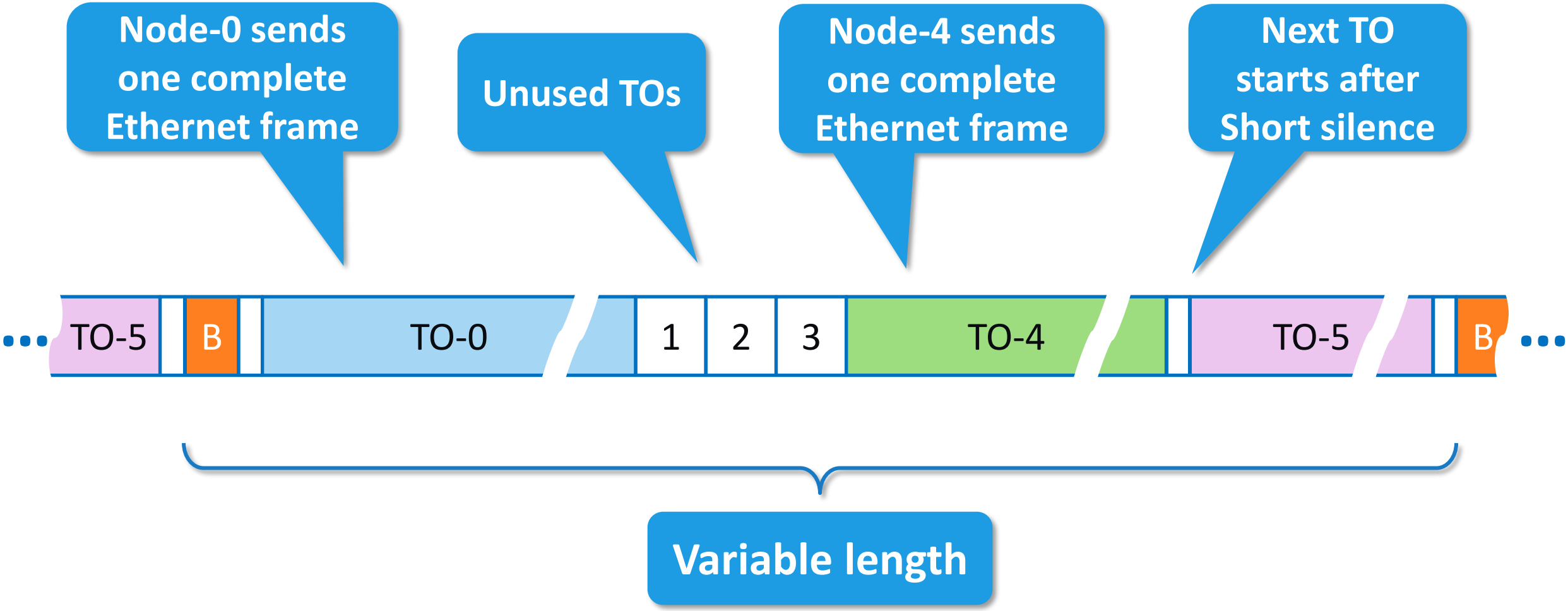
PLCA - Basics



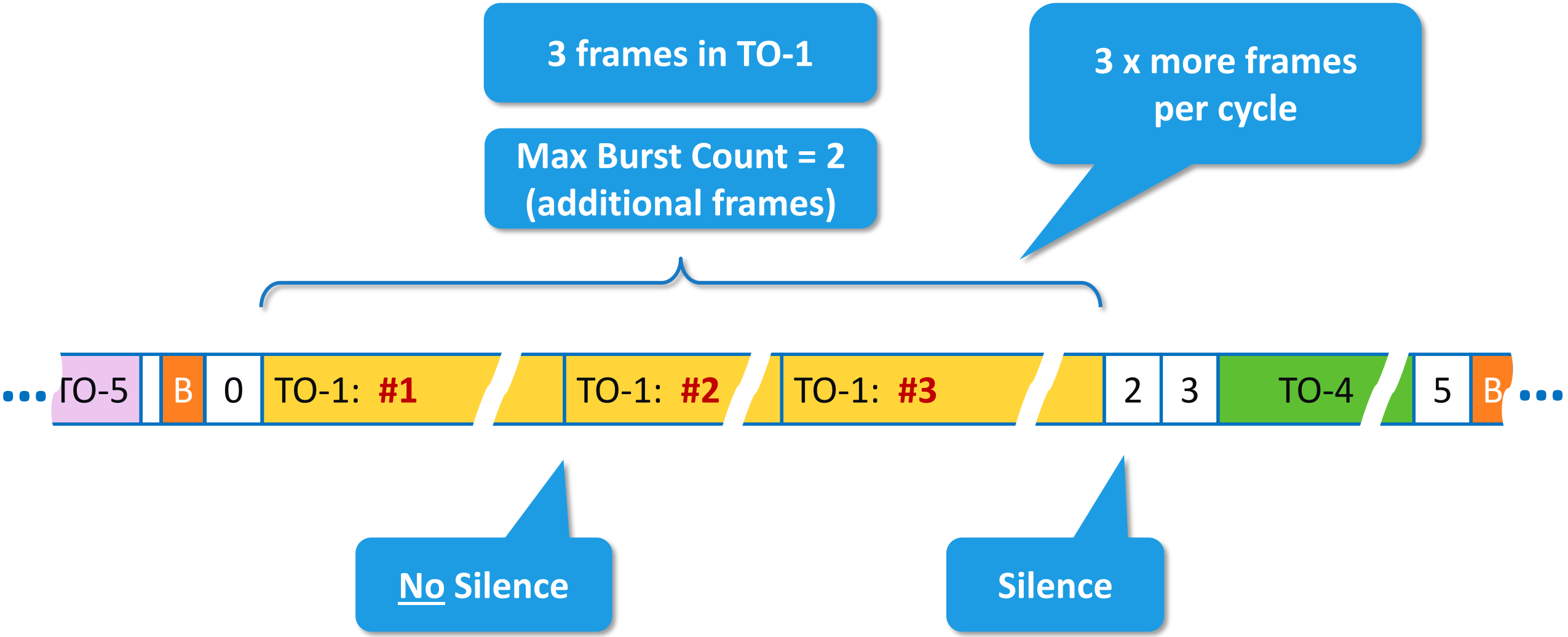
Idle PLCA Bus Cycle / Unpowered Nodes



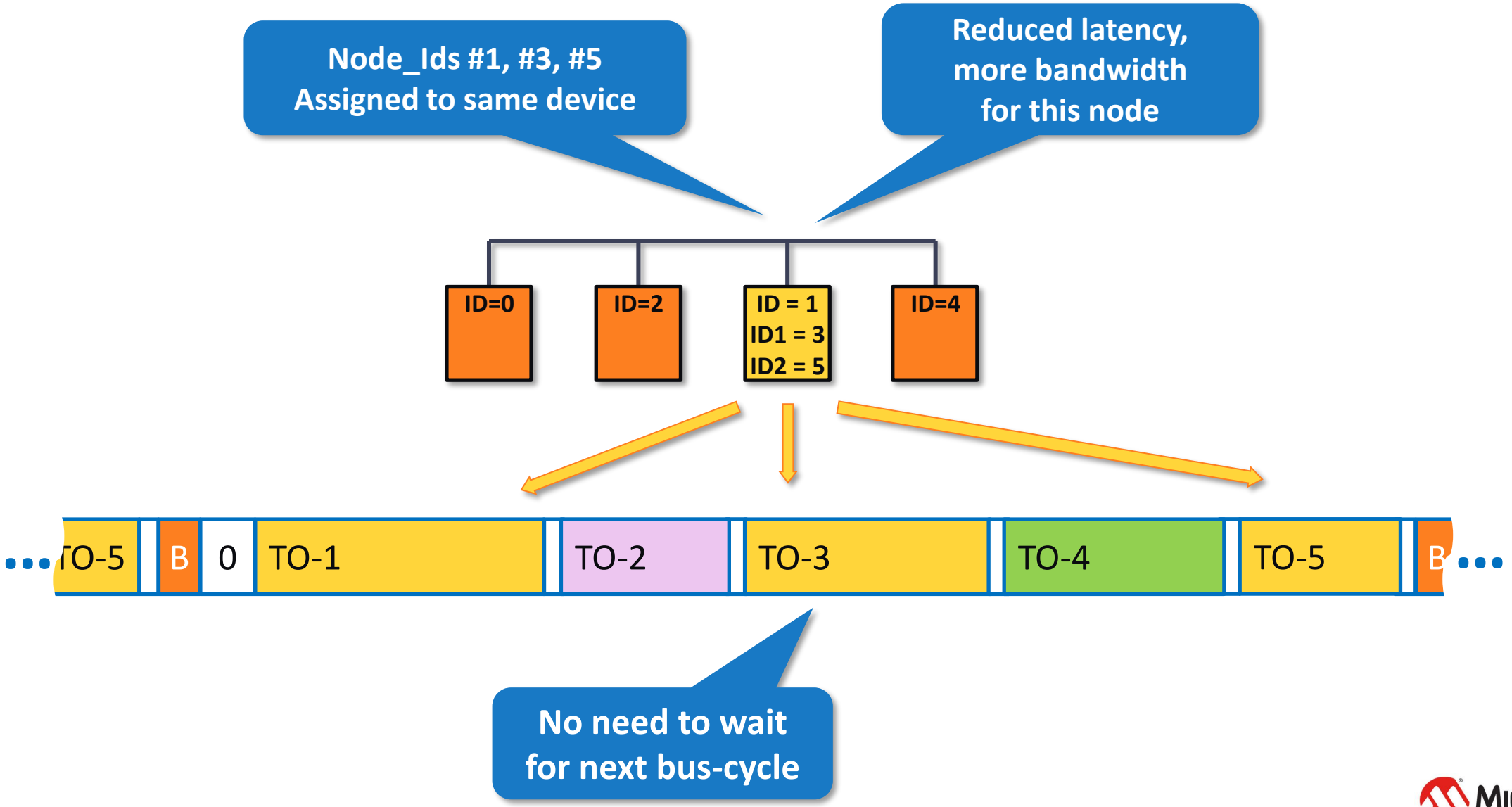
Partly-Filled PLCA Bus Cycle



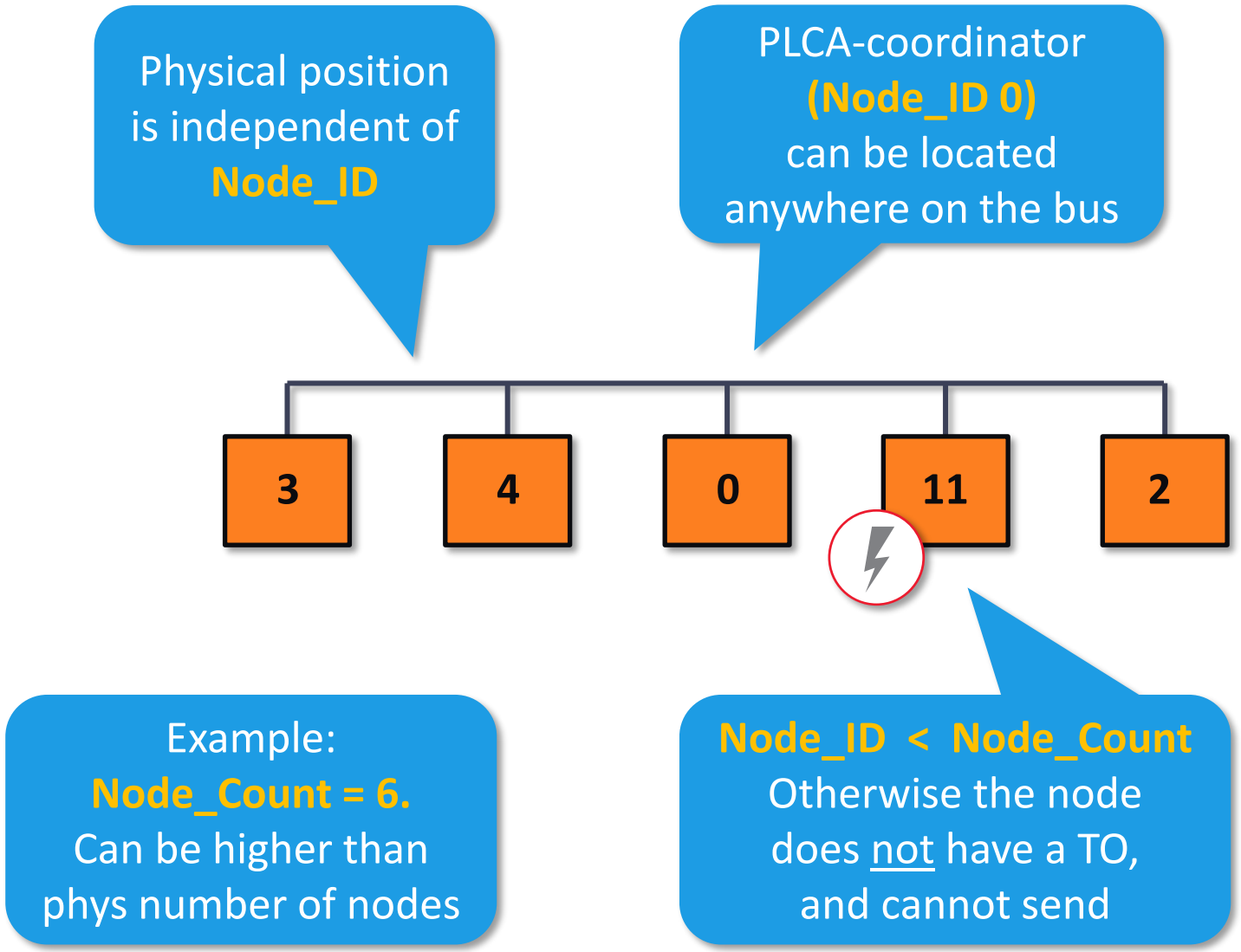
Burst Mode Example



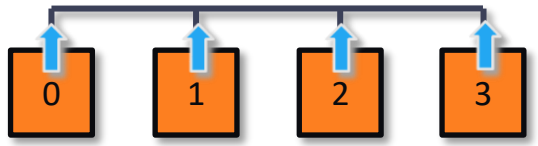
Multiple Transmit Opportunities: Node IDs Example LAN867x / LAN865x



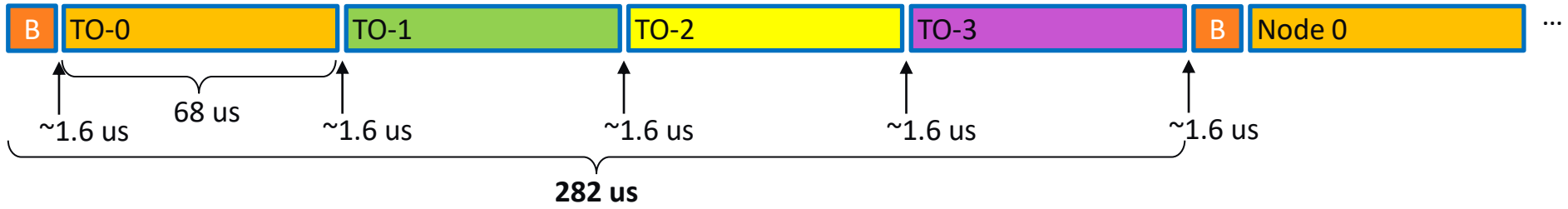
PLCA Configuration



Delay / Latency Examples



- 4-node system, burst mode NOT enabled on any node
- Each node using smallest UDP/Ethernet packet size of 64 bytes
- 46 bytes header, up to 18 bytes of data/commands
- Physical frame = 12B IPG + 64B + 8B preamble + 1B (ESD, ESDOK) = 85 bytes => 85 x 0,8 = 68 us
- Beacon = 20 BT (2 us)
- TO_timer (silence) = 32 BT (3.2 us)
- Short silence = typically 16 BT (1.6 us)
- Length of PLCA bus cycle (in us) = 2 + 4*(1.6 + 68) + 1.6 = 282 us



When each node sends a minimum size packet
=> PLCA bus cycle time = Max delay between two packets of the same node = 282 us

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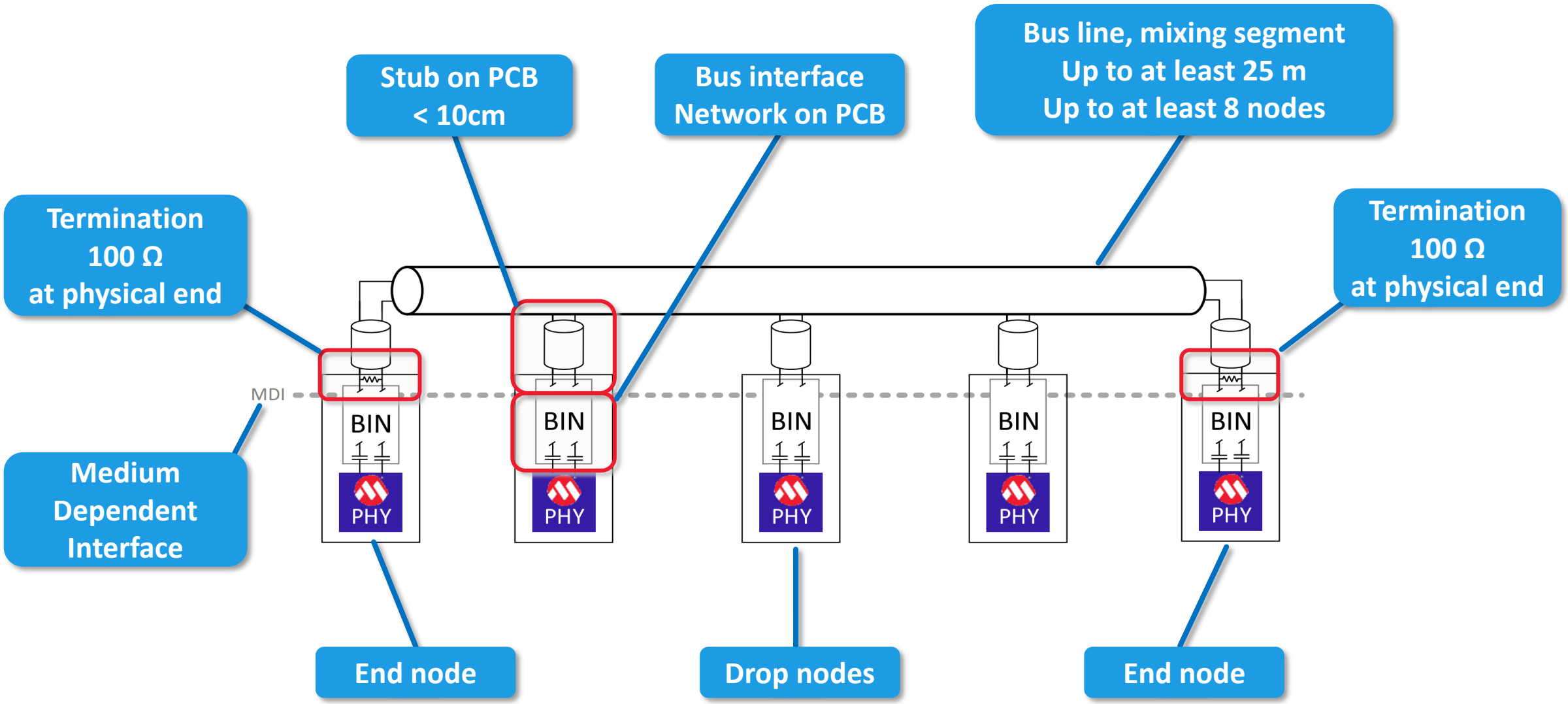
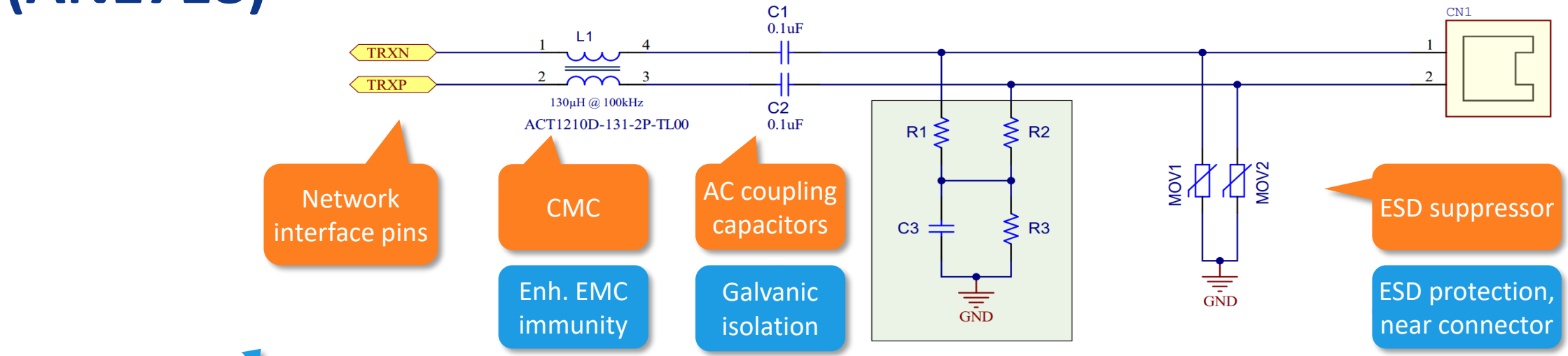
HW Implementation

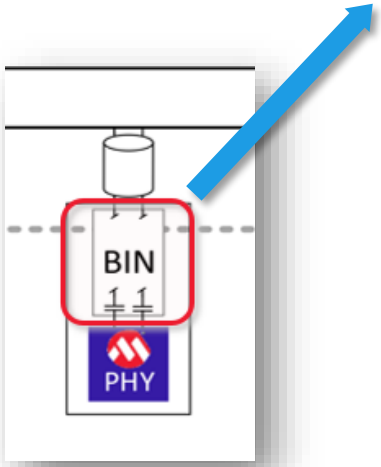
Bus Interface Network

10BASE-T1S Multidrop Bus

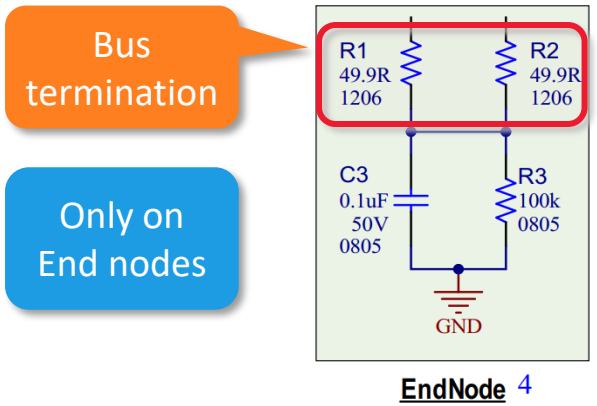


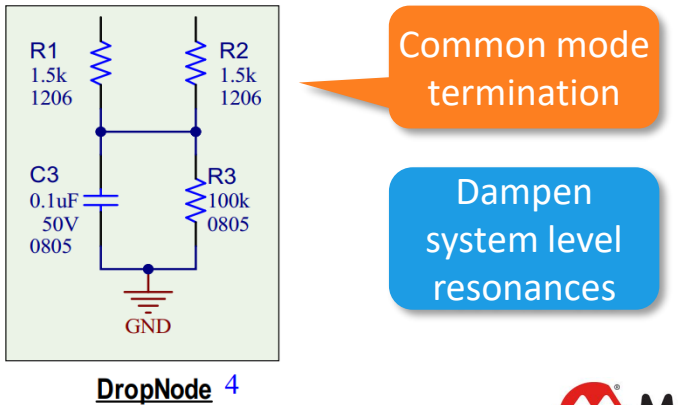
LAN86xx Bus Interface Network (BIN) Reference Design (AN1718)





Please always refer to the latest documentation





Advanced Features

Wake and Sleep

CBS: Credit Based Traffic Shaping

SQI: Signal Quality Indication

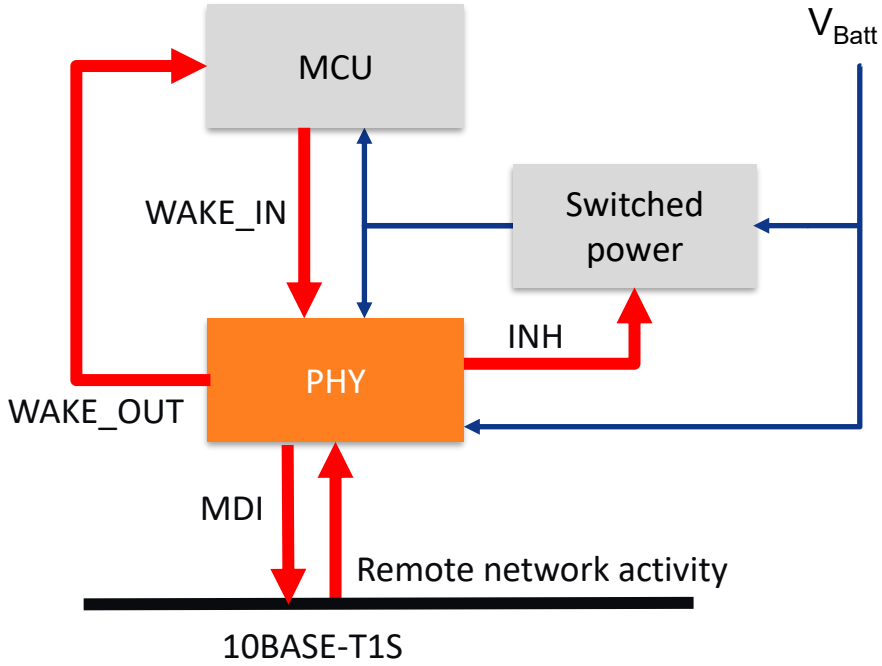
TSN: Time Sensitive Networking

ACMA: Application Controlled Media Access

Wake / Sleep Example

Enables Wake/Sleep on small MCUs without external components according to OPEN Alliance TC10

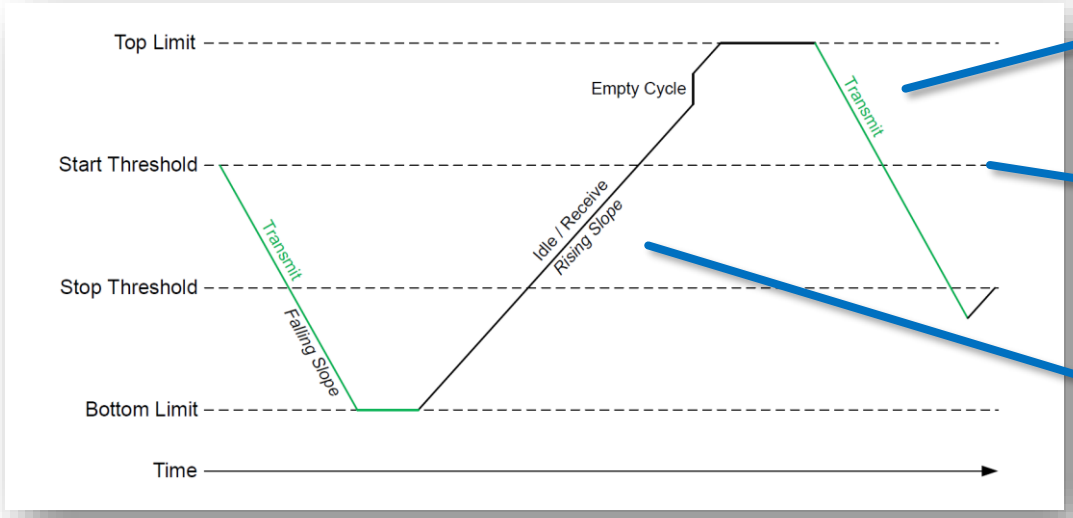
- **Sleep mode**
  - Ultra-low power consumption (<= 140 µW)
  - Just constant 3.3V power supply during sleep, but no switched power
  - Go to sleep via command from host, or via internal watchdog timeout
- **Wake from**
  - Remote network activity (MDI)
  - Local event (WAKE_IN), e.g., user input
- **Activate switched power**
  - INH pin output to enable/disable power supply
- **Forward wake signal**
  - Via MDI (network) to wake remote nodes
  - Via WAKE_OUT to wake other local devices
  - Via WAKE_OUT to inform MCU that network re-assumed operation



CBS – Credit Based Traffic Shaping

- Provides a node a certain bandwidth based on credits
- Prevents a “best-effort-node” from flooding the network
- Bandwidth distribution independent of Ethernet frame length
- HW-based: application only needs to configured
- Works on top of PLCA or CSMA/CD
- Do not mix with PLCA burst mode or cycle skipping

Enables traffic shaping in small MCUs



Credits decrease while TX

Node can only send a packet if it has enough credits

Credits increase while RX or idle

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SQI - Signal Quality Indication

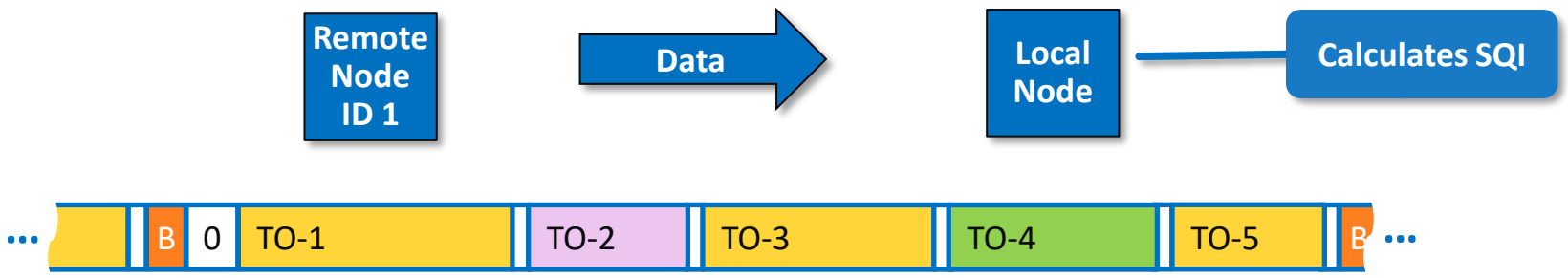
- **LAN867x and LAN865x can accumulate statistics on RX-data**
- **Signal quality of the RX-signal rated in one of 8 levels from 0 (worst) to 7 (best)**
- **MCU can monitor the SQI, detect bad network, detect network degradation over time and take corrective action**

- **Without PLCA:**
  - SQI determined from RX-data from all nodes on the bus

- **PLCA enabled:**
  - SQI determined from RX-data from a single node (transmit opportunity)

Compatible with OPEN Alliance TC14

Advanced diagnostic features for automotive Ethernet PHYs



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Precision Time Protocol

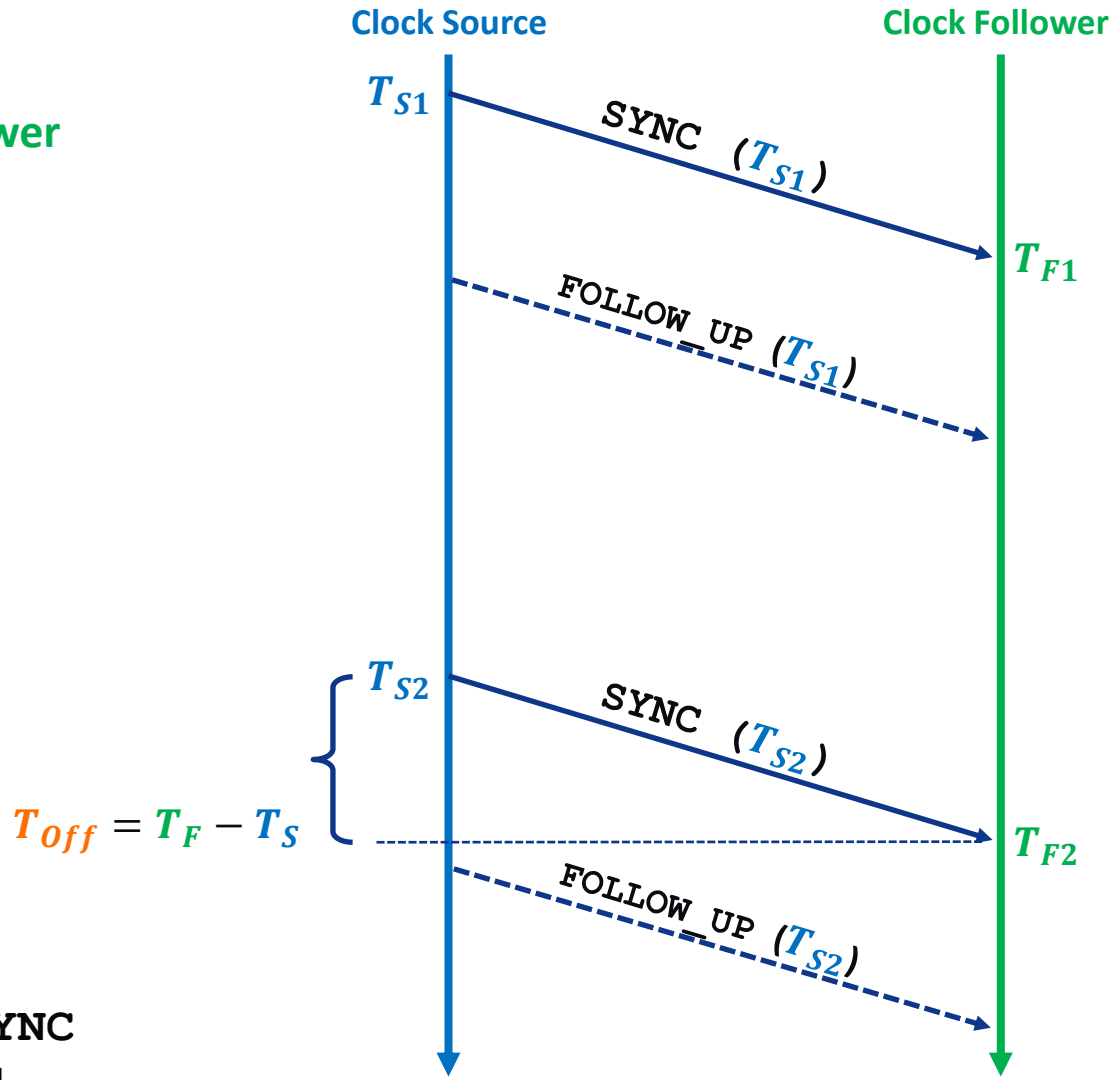
Clock Synchronization

- Independent time domains on **Clock Source** and **Clock Follower**
- **Clock Source** periodically broadcasts a **`SYNC`** message containing its current source time T_S
- **Clock Followers** receive **`SYNC`** at their local time T_F and can calculate offset to the source clock
- Now at any time a follower calculates the source clock with

$$T_S = T_F - T_{off}$$

to use it e.g., for timestamping

- In case a Clock Source can only detect the time of sending **`SYNC`** after sending has been completed, T_S is sent in an additional **`FOLLOW_UP`** message. This two-step-approach is required for gPTP.



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Thank You!