

NORA-B2 series

Stand-alone Bluetooth® Low Energy modules
System integration manual



Abstract

Targeted towards hardware and software engineers, this document describes how to integrate NORA-B2 series stand-alone Bluetooth® Low Energy module in an application product. It explains the hardware design-in, software, component handling, regulatory compliance, and testing of the modules. It also lists the external antennas approved for use with the module.


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This document applies to the following products:

Product name	Document status
NORA-B201	Advance information
NORA-B206	Advance information
NORA-B211	Advance information
NORA-B216	Advance information
NORA-B221	Advance information
NORA-B226	Advance information

 For information about the related hardware, software, and status of listed product types, see also the NORA-B2 data sheet [\[2\]](#).

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1 Product overview

Based on the Nordic nRF54L15, nRF54L10 and nRF54L05 chipset, the NORA-B2 series of small stand-alone modules includes an Arm® Cortex®-M33 processor, with floating-point unit (FPU), digital signal processor (DSP) instruction set, and CryptoCell™-312 security architecture. It also features a 128 MHz RISC-V coprocessor and scalable memory configurations of up to 1.5 MB non-volatile Memory (NVM) and up to 256 KB RAM. All module variants are qualified against Bluetooth® Core 6.0.

NORA-B2 modules support multiple peripherals over high-speed SPI, QSPI, TWI, ADC and PWM interfaces, and include a 2.4 GHz radio capable of handling Bluetooth® Low Energy (LE) and IEEE 802.15.4 short-range wireless radio with Thread®, Matter™ and Zigbee™, and Nordic proprietary protocols. The modules operate at ambient temperatures of up to 85 °C.

NORA-B2 series modules include an internal power management circuitry that requires only a single supply voltage in the range of 1.7–3.6 V. The wide supply range also enhances the suitability of the modules in battery powered systems.

You can integrate several variants into your product, including NORA-B2x1, which has a dedicated pin for connecting an external antenna, or NORA-B2x6, which includes an internal PCB trace antenna.

 Already globally certified for use with an internal antenna or range of external antennas, the time, cost, and effort required to deploy NORA-B2 modules into customer applications is significantly reduced.

For detailed product descriptions of all module variants, see the NORA-B2 data sheet [\[2\]](#).

2 Module integration

NORA-B2 series modules operate as stand-alone (host-less), Open CPU configurations that allow customer applications to run on the module itself – without any need for a supporting host MCU. The modules support Bluetooth® LE and IEEE 802.15.4 wireless radio with Thread®, Matter™ and Zigbee™. NORA-B2 series modules support a wide range of IO interfaces, such as GPIO, UART, SPI, I2C, PWM, I2S, NFC, and QDEC to connect to external peripherals.

Figure 1 shows a typical integration in which NORA-B2 is configured as a host.

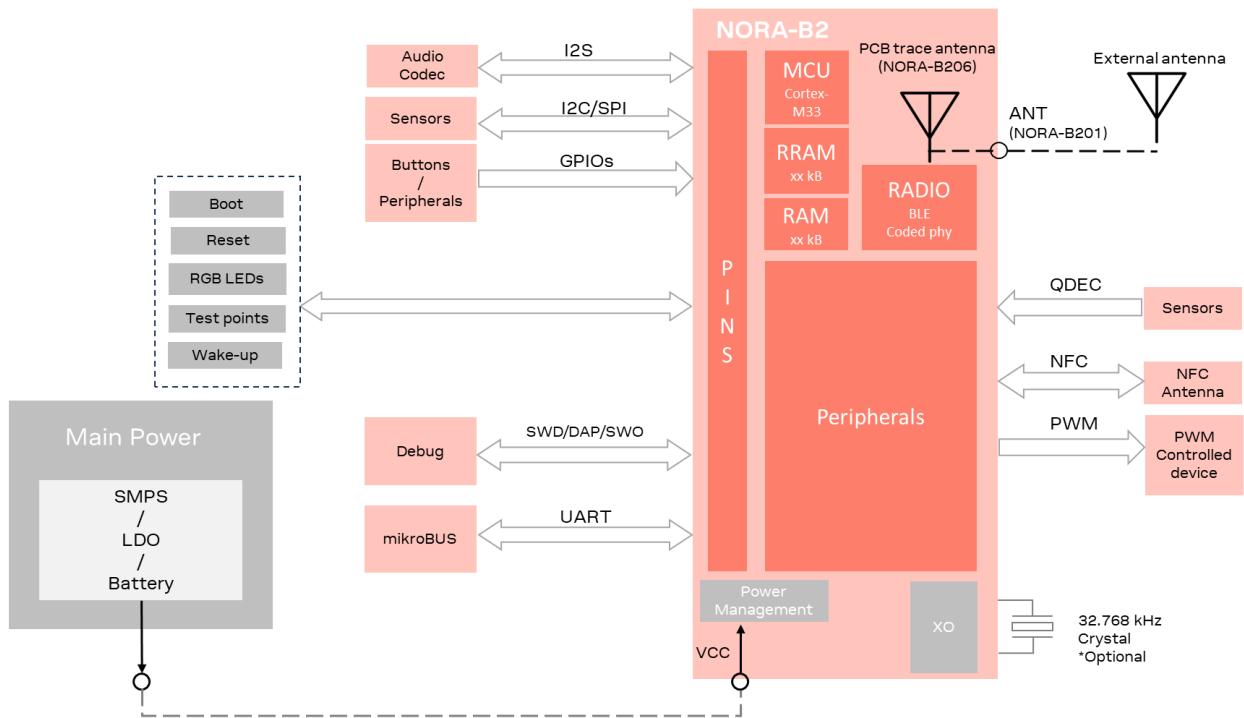


Figure 1: Example of NORA-B2 integrated as a host. RAM and flash size dependent on variant

Figure 2 shows how to control NORA-B2 series modules through a host CPU and interface connections.

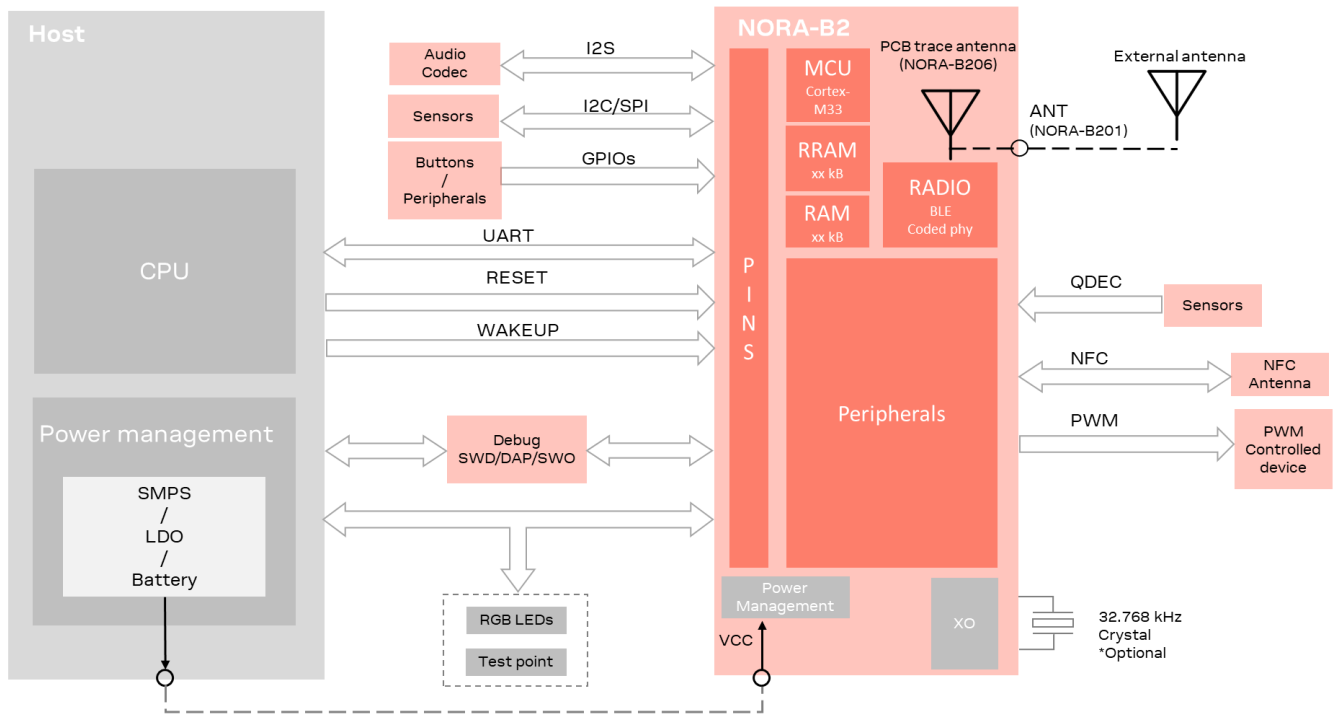


Figure 2: Example of NORA-B2 integration in a host system with external CPU. RAM and flash size dependent on variant

Connect NORA-B2 to a HOST system via UART to add BLE communication capabilities to host application product.

With NORA-B2, application designs are simplified. Developers can either connect an external antenna via the antenna pin on NORA-B2x1 or utilize the internal antenna on NORA-B2x6.

The footprint compatibility with other NORA modules ensures that NORA-B2 series modules offer maximum flexibility for migration enabling use of other radio technologies.

2.1 Power supply

The power for NORA-B2 series modules is applied through the **VCC** pin.

The internal power and clock management system monitors the SoC's components power and clock requests to operate the lowest power consumption mode.

2.1.1 VCC application circuits

Although NORA-B2 includes a complete power management system and can be sourced from a battery, an external regulator might be required. Then the supplies are taken from either of the following sources:

- Switching Mode Power Supply (SMPS)
- Low Drop Out (LDO) regulator

An SMPS is the ideal design choice when the available primary supply source is significantly higher than the operating supply voltage of the module. This offers the best power efficiency for the application design and minimizes the amount of current drawn from the main supply source.

- ⚠** When taking VCC supplies from an SMPS, make sure that the AC ripple voltage is kept as low as possible at the switching frequency. Design layouts should focus on minimizing the impact of any high-frequency ringing.

Use an LDO linear regulator for primary VCC supplies that have a relatively low voltage. As LDO regulators dissipate power linearly related to the step-down voltage, LDOs are not recommended for the step down of high voltages.

DC/DC efficiency should be regarded as a trade-off between the active and idle duty cycles of an application. Although some DC/DC devices achieve high efficiency at light loads, these efficiencies typically degrade as soon as the idle current drops below a few milliamps. This can have a negative impact on the life of the battery.

If decoupling capacitors are needed on the supply rails, it is best practice to position these as close as possible to the NORA-B2 series module. The power routing of some host system designs makes decoupling capacitance unnecessary.

For electrical specifications, see NORA-B2 series data sheet [\[2\]](#).

2.2 System functions

2.2.1 Power modes

NORA-B2 series modules support the following power modes:

- *System ON*
- *System ON low power - Default*
- *System ON IDLE sub-modes*
- *System OFF*

In system on IDLE mode, NORA-B2 run in one of the sub modes Constant latency or Low-power mode. Constant latency provides a predictable CPU latency at the cost of increased current consumption. Low-power mode provides lowest possible power consumption.

For a detailed description of each power mode, see also the NORA-B2 data sheet [\[2\]](#).

2.2.2 Module reset

NORA-B2 series module is reset / rebooted through the **RESET_N** pin:

- **RESET_N** has an internal pull-up resistor that sets its default state to high. Setting the pin low triggers a “hardware reset” of the module.
- **RESET_N** is preferably driven by either an open-drain or open-collector output or a contact switch.

NORA-B2 series modules can also be reset using other methods. For more information, see also NORA-B2 data sheet [\[2\]](#).

2.2.3 Global Real Time Clock (GRTC)

The LFCLK oscillator control, included in the module’s chip, manages the low frequency clock sources and requests.

When peripherals require a low frequency clock, LFCLK, for watchdog timer, or global real-time counter (GRTC). This is provided by the LFCLK control system. The LFCLK is generated from either of the following sources:

- RC oscillator, LFRC, included in the chip
- Crystal oscillator, LFXO, with an external oscillator connected to pin B6 and C6.
- Synthesized by the LFSYNT from the high frequency clock, HFCLK.

The LFCLK source is selected by the LFCLK.SRC register. If LFXO is selected, it initially starts with the LFRC and switch to LFXO once the oscillator is stable.

An external crystal provides the lowest sleep current consumption. Although the 32 kHz LFRC consumes slightly more sleep current, it provides a leaner Bill of Materials (BOM).



For RTC pinout information, see also NORA-B2 data sheet [2].

2.2.3.1 Internal oscillator - 32 kHz LFRC

Using the embedded 32 kHz low-frequency RC oscillator (LFRC) as the module clock provides a more cost-effective Bill of Materials (BoM), lowering costs for end users. However, this choice may result in a slight increase in power consumption.

If you choose to source the module clock from the LFRC, pins 1 and 2, **P1.00/XL1**, **P1.01/XL2** can be assigned as GPIOs.

2.2.3.2 External crystal

In addition to the embedded 32 kHz low-frequency RC oscillator (LFRC), developers can use an external 32.768 kHz low-frequency crystal oscillator (LFXO) with NORA-B2 series modules to achieve the lowest overall power consumption. To enable this oscillator in your application, connect it to pins 1 and 2 (P1.00/XL1 and P1.01/XL2). The NORA-B2 series datasheet provides the specifications for the optional LFXO.

[Table 1](#) describes the specification of the crystal used on EVK-NORA-B2. Note that the 32 kHz crystal is not mounted on EVK-NORA-B2.

Component	Value	Note
Crystal	32.768 kHz – 20 ppm	AVX KYOCERA ST3215SB32768E0HPWZZ used on EVK-NORA-B2

Table 1: Specification of the low-frequency crystal used on the EVK-NORA-B2 evaluation kit

2.3 Antenna integration

NORA-B2 series modules support either an internal antenna in NORA-B2x6 or external antennas connected through a dedicated antenna pin in NORA-B2x1.

2.3.1 Antenna solutions

NORA-B2 series modules support three different antenna solutions:

- NORA-B201 includes an antenna pin to connect an external antenna to the NORA-B201 module. The antenna can be either:
 - An antenna external to the end product – typically used in end products with a metal enclosure.
 - An antenna external to the NORA-B2x1 module but internal to the end product. Examples of this include a chip antenna on the host PCB or a flex film antenna.
- NORA-B206 is equipped with an internal PCB trace antenna that is custom-designed and optimized for the module. With this configuration, there's no requirement for an RF trace design on the host PCB – which means less effort during the host PCB design and testing in the lab.

Figure 3 provides a summary of all the available antenna options.

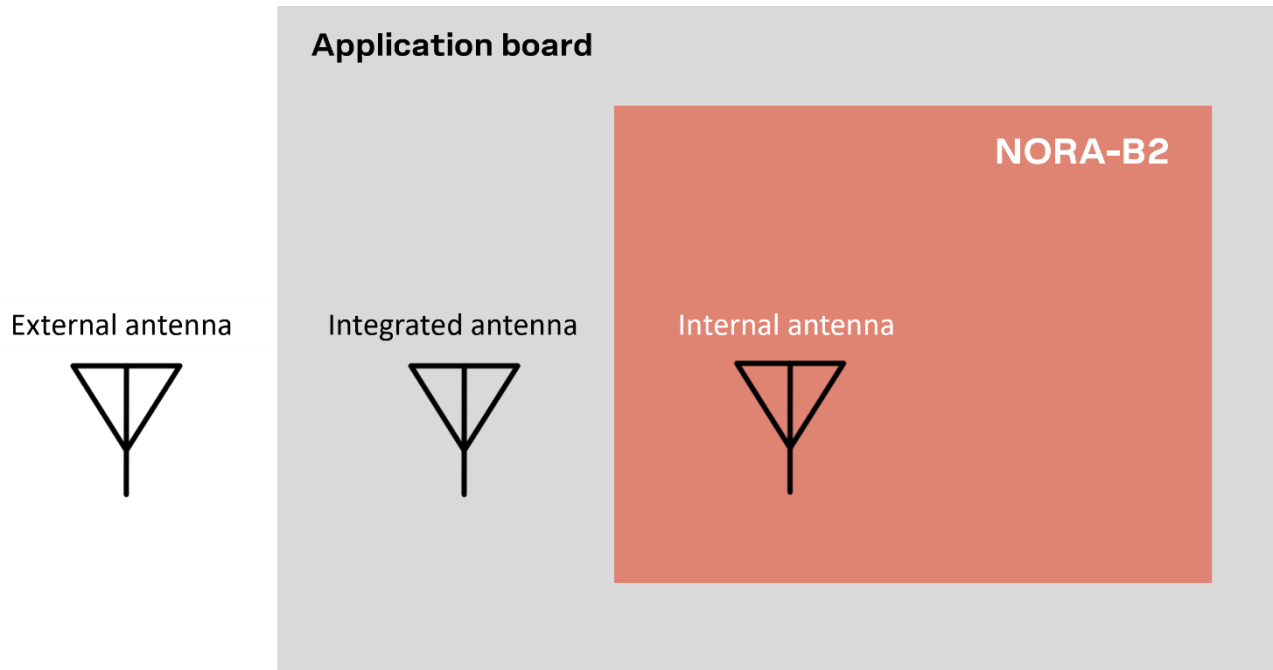


Figure 3: Antenna options

- External antenna: An external antenna of choice connected through a coaxial cable to an U.FL or Reverse Polarity SMA connector placed on the application PCB and connected to the module antenna pin.
- Integrated antenna: A permanent antenna included in the PCB application design. Ideally an SMD antenna mounted on the application PCB or a Flexible PCB antenna attached to the application product housing.
- Internal antenna: An antenna embedded on the module. Integrated the module according with instruction to reach optimum antenna performance.

2.3.2 Approved antenna designs

NORA-B2 series modules come with a pre-certified design that can significantly reduce costs and save time during the certification process. To leverage this benefit, customers must implement an antenna layout that fully complies with the u-blox reference design outlined in [Appendix B](#). Reference design source files – available from u-blox on request.¹

Designers integrating a u-blox reference design into an end-product assume sole responsibility for any unintentional emission levels produced by the end product.

For Bluetooth operation, NORA-B2 series modules have been tested and approved for use with the antennas listed in the [pre-approved antennas list](#).

- ⚠ To ensure that the compliance and pre-certification of u-blox modules with the various regulatory bodies remains valid, use only the external antennas listed in the [pre-approved antennas list](#). Reference design source files are available from u-blox on request.
- ⚠ If the module is integrated with other antennas, the OEM installer must certify the design with respective regulatory agencies.

¹ Reference design files are made available only after certification

2.4 Data interfaces

NORA-B2 supports five serial interfaces with EasyDMA, including UART, I2C, I2S, and SPI controller/peripheral.


2.4.1 Universal Asynchronous Receiver/Transmitter (UART)

NORA-B2 series modules include a UART interface for data communication and firmware upgrade. The UART can continue operating while the processor is in low-power mode if an appropriate peripheral clock is available.

The UART supports the following signals:

- Data lines (**RXD** as input, **TXD** as output)
- Hardware flow control lines (**CTS** as input, **RTS** as output)

The UARTs can be used in 4-wire mode with hardware flow control, or in 2-wire mode with **TXD** and **RXD** only.

 2-wire mode is not recommended as it is prone to buffer overruns.

The IO level of the UARTs follows **VCC**.

2.4.2 Serial peripheral interface (SPI)


NORA-B2 supports a Serial Peripheral Interface (SPI) interface.

Main and *Sub* node operations are possible on the interface.

The LPSPI interfaces use the following signals:

Signal name	Description
LPSPiX_SCK	Serial clock output, up to 24 MHz
LPSPiX_SIN	MISO serial input data/ Data 1 I/O signal
LPSPiX_SOUT	MOSI serial output data/ Data 0 I/O signal

Table 2: LPSPI signals in Main mode

 For an external storage example and pin assignment information, see also the NORA-B2 data sheet [2].

2.4.3 Inter-Integrated Circuit (I2C)

NORA-B2 series modules include a two-wire Interface which is I2C interface compatible.

The I2C interfaces can operate as Controller with multiple *Target* devices on the I2C bus and support standard-mode (100 kbps), 250 kbps, fast-mode (400 kbps), and fast-mode plus (1 Mbps) operation.

The interface uses the **SCL** signal to clock instructions and data on the **SDA** signal.

- I2C 2-wire pin configuration:
 - SCL - Clock output in *Controller* device and input in *Target* device
 - SDA - Data input/output pin

The I2C interface requires external pull-up resistors. These shall be connected to the same voltage as the IO voltage of the NORA-B2. The pull up resistor value you choose depends on the number of devices connected to the bus, the total capacitive load, and the interface speed selected. With a single device connected, 8– 10 kΩ is recommended. Use a smaller value if more devices are connected.

It is recommended that you verify the interface signal performance to decide optimum resistor value.

2.4.4 Inter-IC Sound interface (I2S)

NORA-B2 includes an I2S interface with two-channel format and left- and right-aligned formats.

Simultaneous bidirectional audio streaming

- Original I2S and left- or right-aligned formats
- 32-, 24-, 16-, and 8-bit sample widths
- Separate sample and word widths
- Low jitter

2.5 Other Digital interfaces

2.5.1 Near Field Communication (NFC)

NORA-B2 includes a Near Field Communication Tag (NFCT) that is compliant with listening device NFC-A. The NFCT peripheral contains a 13.56 MHz AM receiver and a 13.56 MHz load modulator with 106 kbps data rate.

Connect an inductive NFC antenna to NORA-B2 pins C5 (NFC1) and B5 (NFC2) and use tuning capacitors to achieve resonance at 13.56 MHz.

The reader and tag are magnetically coupled with each other. The energy transferred depends on the antenna tuning, the size of the antennas, and antenna orientation.

If a specific operating distance is desired these parameters must be considered.

2.5.2 Pulse Width Modulation (PWM)

NORA-B2 modules support three pulse width modulators with up or up-down counters and four PWM channels that drive assigned GPIOs.

The counter, compare, and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes.

2.5.3 Quadrature Decoder (QDEC)

NORA-B2 includes two quadrature decoders (QDEC)

Each QDEC is used to read quadrature encoded data from mechanical and optical sensors in the form of digital waveforms. Quadrature encoded data is often used to indicate rotation of a mechanical shaft in either a positive or negative direction.


The QDECs have two inputs, channel 0 (PHASE_A) and channel 1 (PHASE_B), to control incremental and decremental counting in the Timer/PWM Module (TPM). Each QDEC supports two encoding modes: count and direction encoding mode and phase encoding mode. See also [Timer/PWM Module \(TPM\)](#).

The TPM counter is clocked by channel 0 and channel 1 input signals when the quadrature decoder mode is selected. Therefore, in quadrature decoder mode, channel 0 and channel 1 can only be used in software compare mode. Other TPM channels can only be used in input capture or output compare modes.

2.6 Analog interfaces

NORA-B2 has up to 31 GPIOs, 8 of which have analog input pins supporting the following functions:

- 8/10/12-bit Analog to Digital Converter (ADC) with up to eight programmable gain channels
- Comparator (COMP)
- 1x Voltage reference (Vref)

 For more information about ADC, LPCMP and VREF, see also the NORA-B2 data sheet [2].

2.7 Debug interfaces

2.7.1 SWD

NORA-B2 series modules provide a 2-pin, serial-wire, debug interface with a clock (**SWDCLK**) and a single bi-directional data pin (**SWDIO**) for debug and test functionality.

Pin name	SWD		Internal pull-up/pull-down
	Type	Description	
SWDCLK	I	Clock	Pull-down
SWDIO	I/O	Data	Pull-up

Table 3: SWD signals

2.7.2 DAP

NORA-B2 series modules provide a Debug Access Port (DAP) to debug and trace the core system of the module. On NORA-B2 series modules, the SWD interface is used as the external connection interface of DAP.

2.7.3 SWO

NORA-B2 supports a 1-bit Serial Wire Output (SWO) trace port for efficiently accessing core trace information from outside of the module. The SWO port is used to stream-out trace information from various parts of the module, including the Data Watchpoint and Trace (DWT) part, Instrumentation Trace Macrocell (ITM) part, and Breakpoint Unit (BPU) part.

2.8 NORA migration

The NORA-B2 module shares the same mechanical outline and footprint as other modules in the NORA family. When designing for migration, pay special attention to the following:

Power Supply

- The NORA-B2 power supply is connected to the same pins as the generic NORA family pinout.
- Ensure the supply voltage and current consumption match the figures stated in the datasheet.
- NORA-B2 operates with a supply voltage ranging from 1.7 to 3.5 V.
- The interface voltage for NORA-B2 is set by **VCC**.
- For migration, use LDOs or switched-mode DC/DC regulators from standard series to easily adjust the power supply to match the module.

Control Signals

- NORA-B2 uses a power-down signal, **RESET_N**, positioned on a generic pin position and includes a generic pull-up resistor.
- NORA-B2 has a unique **WAKE-HOST** signal located on pin E8.

Flashing and Debug

- The SWDIO/SWDCLK interface is located on common pins.
- Debugging interfaces are available on pins A5 (TX) and A6 (RX).

Antenna Connection

- NORA-B2 uses the generic NORA family pin for antenna connection.

3 Design-in

Follow the design guidelines in this chapter to optimize the integration of NORA-B2 series modules in the final application board.


3.1 Overview

All application circuits must be properly designed, but several points require special attention during the application design. In an order of importance consider:

- Module antenna connection: **ANT** pad RF transmission lines connecting the **ANT** pad with the related antenna connector or antenna, must be designed with a 50 Ω impedance characteristic. See also [RF transmission line design](#).
- Module supply: **VCC** pin.
Supply circuits can affect RF performance, so it is important to observe the schematic and layout design for these supplies. See also [VCC application circuits](#). Select appropriate power supply source and bypass capacitors, and then carefully route the power supply nets or planes. Modules normally include several supply pins described in the pinout of the NORA-B2 series data sheet [2].
- High-speed interfaces: **UART, SPI, I2C** pins.
High-speed interfaces are a potential source of radiated noise that can affect the regulatory compliance standards for radiated emissions. It is important to follow the schematic and layout design recommendations described in the [General layout guidelines](#).
- System functions: **RESET_N**, GPIO, and other System input and output pins
Careful utilization of these pins in the application design is required to guarantee for correct boot up and system operation. Ensure that the voltage level is correctly defined during module boot. It is important to follow the schematic and layout design recommendations described in the [General layout guidelines](#).
- Other pins: **ADC, I2S, QDEC**, and NC pins.
Careful utilization of these pins is required to guarantee proper functionality. It is important to follow the schematic and layout design recommendations described in the [General layout guidelines](#).

3.2 RF interface

As the module must be strategically mounted, careful consideration should be given to its placement to avoid interference with radio communication. NORA-B2x6 modules include an internal PCB trace antenna, which makes them unsuitable for mounting in a metal enclosure. No metal casing or plastics using metal flakes should be used. Avoid metallic based paint or lacquer as well. NORA-B2x1 modules offer more freedom as an external antenna can be mounted further away from the module.

-  According to the FCC regulations, the transmission line from the module antenna pin to the antenna or antenna connector on the host PCB is considered part of the approved antenna design. Therefore, module integrators must either follow one of the antenna reference designs used in the module's FCC type approval exactly or certify their own designs.

3.2.1 Antenna integration

At the start of the application design phase, when the mechanical design and the physical dimensions of the board are still under analysis/decision, the antenna integration shall be considered. Apart from the product's performance, the compliance and subsequent certification of the RF design depends heavily on the radiating performance of the antennas. Note also that the RF certification of the module is extended through to the application design.

Adhere to the following guidelines to ensure proper performance of the application product:

- External antennas, including, linear monopole classes:
 - Place the module and antenna in any convenient area on the board. External antennas don't impose any restriction on where the module is placed on the PCB.
 - Select antennas with an optimal radiating performance in the operating bands. The radiation performance depends mainly on the antennas.
 - Choose RF cables that offer minimum insertion loss. Unnecessary insertion loss is introduced by low quality or long cables. Large insertion losses reduce radiation performance.
 - Use a high-quality 50 Ω coaxial connector for proper PCB-to-RF-cable transition.
- Integrated antennas, such as patch-like antennas:
 - Internal integrated antennas impose some physical restrictions on the PCB design. Given that the orientation of the ground plane related to the antenna element must be considered:
 - Integrated antennas excite RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna; its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced to a minimum size that should not be smaller than a quarter of the wavelength of the minimum frequency that is to be radiated.
 - Find a numerical example to estimate the physical restrictions on a PCB, where:
Frequency = 2.4 GHz → Wavelength = 12.5 cm → Quarter wavelength = 3.5 cm in free space or 1.5 cm on a FR4 substrate PCB.
- Choose antennas with optimal radiating performance in the operating bands. Radiation performance depends on the complete product and antenna system design, including the mechanical design and usage of the product. [Table 4](#) summarizes the requirements for the antenna RF interface.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the ANT pin.
Frequency Range	2400 - 2500 MHz	Bluetooth Low Energy.
Return loss	$S_{11} < -10$ dB (VSWR < 2:1) recommended $S_{11} < -6$ dB (VSWR < 3:1) acceptable	The return loss or S_{11} . As a parameter of the of the standing waves ratio (VSWR) measurement, S_{11} refers to the amount of reflected power. This parameter indicates how well the primary antenna RF connection matches the 50 Ω characteristic impedance of the ANT pin. To maximize the amount of the power transferred to the antenna, the impedance of the antenna termination must match (as much as possible) the 50 Ω nominal impedance of the ANT pin over the entire operating frequency range.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	Radiation efficiency is the ratio of the radiated power against the power delivered to the antenna input; the efficiency is a measure of how well an antenna receives or transmits.
Maximum Gain	+3 dBi	Although higher gain antennas can be used, these must be evaluated and/or certified. To comply with regulatory agencies radiation exposure limits, the maximum antenna gain must not exceed the value specified in the data sheet [2] . See also Regulatory compliance .

Table 4: Summary of antenna interface requirements for NORA-B20

3.2.2 RF transmission line design

RF transmission lines connecting the **ANT** pad with the related antenna connector or antenna, must be designed with a $50\ \Omega$ impedance characteristic.


Figure 4 shows the design options for PCB transmission lines, where:

- Microstrip – trace coupled to a single ground plane, separated by dielectric material.
- Coplanar microstrip – trace coupled to ground plane and adjacent conductors, separated by dielectric materials).
- Stripline – track separated by dielectric material and sandwiched between two parallel ground planes.

The parameters shown in the cross-sectional area of each trace design include:

- Width (W) – shows the width of the copper layer on the top layer
- Distance (S) – shows the distance between the top copper layer and the two adjacent GND planes.
- Dielectric substrate thickness (H) – shows the distance between the GND reference on the bottom plane and the copper layer on the top layer.
- Thickness of the copper layer (T) – can also be represented by “Base Copper Weight”, which is commonly used as the parameter for PCB stack-up.

Dielectric constant (ϵ_r) defines the ratio between the electric permeability of the material against the electric permeability of free space.

 The width of a $50\ \Omega$ microstrip depends on mainly “ ϵ_r ” and “ H ”, which must be calculated for each PCB layer stack-up.

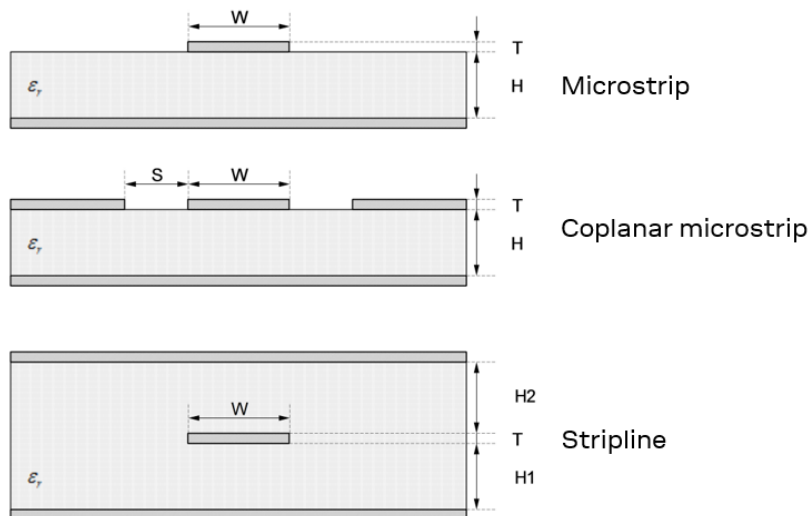


Figure 4: Transmission line trace design

Follow these recommendations to design a $50\ \Omega$ transmission line correctly:

- The designer should provide enough clearance from surrounding traces and ground in the same layer. In general, a trace to ground clearance of at least two times the trace width should be considered. The transmission line should also be “guarded” by ground plane area on each side.
- The characteristic impedance can be calculated as first iteration using tools provided by the layout software. It is advisable to ask the PCB manufacturer to provide the final values that are usually calculated using dedicated software and available stack-ups from production. It could also be possible to request an impedance coupon on panel’s side to measure the real impedance of the traces.

- FR-4 dielectric material, despite its high losses at high frequencies, can be considered in RF designs – provided that:
 - RF trace length must be minimized to reduce dielectric losses.
 - If traces longer than a few centimeters are needed, the use of a coaxial connector and cable to reduce losses is recommended.
 - Stack-up should allow for thick 50 Ω traces and at least 200 μm trace width is recommended to assure good impedance control over the PCB manufacturing process.
 - FR-4 material exhibits poor thickness stability and thus less control of impedance over the trace length. Contact the PCB manufacturer for specific tolerance of controlled impedance traces.
- The transmission lines width and spacing to the GND must be uniform and routed as smoothly as possible: route RF lines in 45 °C angle or in arcs.
- Add GND stitching vias around transmission lines.
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough vias on the adjacent metal layer.
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit to avoid crosstalk between RF traces and Hi-impedance or analog signals.
- Avoid stubs on the transmission lines, any component on the transmission line should be placed with the connected pad over the trace. Also avoid any unnecessary component on RF traces.

3.2.3 NORA-B2x1

NORA-B2x1 is suited for designs that, due to mechanical integration or placement of the module, require an external antenna.

At the beginning of the design phase, when the physical dimensions of the application board are under analysis/decision, designers must take care of the antennas from all perspectives. RF compliance of the device, integrating NORA-B2x1 module with all the applicable required certification schemes, heavily depends on the radiating performance of the antennas. Designers are encouraged to consider one of the u-blox suggested antennas and follow the layout requirements.

3.2.3.1 RF connector design

If an external antenna is required, designers should use a proper RF connector. It is the responsibility of the designer to verify the compatibility between plugs and receptacles used in the design.

[Table 5](#) suggests several RF connector plugs that designers can use to connect RF coaxial cables based on the declaration of the respective manufacturers.

Manufacturer	Series	Remarks
Hirose	U.FL® Ultra Small Surface Mount Coaxial Connector	Recommended
I-PEX	MHF® Micro Coaxial Connector	
Tyco	UMCC® Ultra-Miniature Coax Connector	
Amphenol RF	AMC® Amphenol Micro Coaxial	
Lighthorse Technologies, Inc.	IPX ultra micro-miniature RF connector	


Table 5: U.FL compatible plug connector

The Hirose U.FL-R-SMT RF receptacles (or similar parts) require a suitable mated RF plug from the same connector series. Due to wide usage of this connector, several manufacturers offer compatible equivalents. It is the responsibility of the designer to verify the compatibility between plugs and receptacles used in the design.

Typically, the RF plug is available as a cable assembly. Different types of cable assemblies are available, and the user should select the cable assembly best suited for the application. The key characteristics of an appropriate plug include:

- RF plug type: Select U.FL or equivalent
- Nominal impedance: 50 Ω
- Cable thickness: Select thicker cables – typically those with a thickness between 0.8 mm to 1.37 mm, to minimize insertion loss.
- Cable length: The standard cable length is typically 100 mm or 200 mm; custom lengths are available on request. Select shorter cables to minimize insertion loss.
- RF connector terminating the other side of the cable: for example, another U.FL (for board-to-board connection) or SMA (for panel mounting).

SMT connectors are typically rated for a limited number of insertion cycles. In addition, the RF coaxial cable may be relatively fragile compared to other types of cables. To increase application ruggedness, connect the U.FL connector to a more robust connector such as SMA fixed on panel.

 A de-facto standard for SMA connectors suggests that the usage of reverse polarity connectors (RP-SMA) on Wi-Fi and Bluetooth end products make it more difficult for end users to replace the antenna with higher gain versions that exceed regulatory limits.

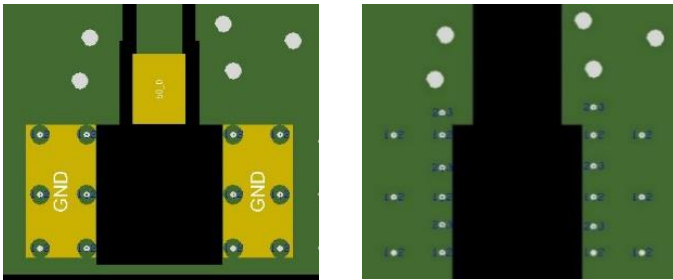


Figure 5: U.FL connector layout showing top layer (left) and inner layer 1 (right)

Strictly follow the connector manufacturer's recommended layout:

- SMA Pin-Through-Hole connectors require a void GND keep-out clearance area on all the layers around the central pin – up to annular pads of the four GND posts.
- UFL surface mounted connectors require no conductive traces in the area below the connector between the GND land pads.

If the connector's RF pad size is wider than the microstrip, remove the GND layer beneath the RF connector to minimize the stray capacitance and keep the RF line to an impedance of 50 Ω . To reduce parasitic capacitance-to-ground for example, the active pad of the U.FL. connector must include (at the very least) a void GND keep-out clearance area on the first inner layer.

3.2.3.2 Integrated antenna design

If integrated antennas are used, the transmission line is terminated by the integrated antennas themselves. Observe the following guidelines:

- The antenna design process should begin at the start of the whole product design process. Self-made PCBs and antenna assemblies are useful for estimating the overall efficiency and radiation path of the intended design.
- Use antenna manufacturer designs that provide the best possible return loss (or VSWR).
- Provide a ground plane large enough according to the related integrated antenna requirements. The ground plane of the application PCB may be reduced to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated; however overall antenna efficiency may benefit from larger ground planes.

- Proper placement of the antenna and its surroundings is also critical for antenna performance. Avoid placing the antenna close to conductive or RF-absorbing parts, such as metal objects and ferrite sheets, as these may absorb part of the radiated power, shift the resonant frequency of the antenna, or otherwise affect the antenna radiation pattern.
- Strict adherence to the guidelines from antenna manufacturer is recommended. Consider carefully regarding their instructions for correctly installing and deploying the antenna system, including the design of the PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require tuning/matching to comply with all the applicable required certification schemes. It is recommended that you plan measurement and validation activities with the antenna manufacturer before releasing the end-product to manufacturing.
- RF parts may be affected by noise sources like hi-speed digital buses. Avoid placing the antenna close to buses such as a Double Data Rate (DDR) bus and consider taking specific countermeasures like metal shields or ferrite sheets to reduce interference.

3.2.4 NORA-B2x6

NORA-B2x6 modules include an internal PCB trace antenna that is integrated on the module PCB using antenna technology from Abracon. The RF signal is completely internal and not connected to any module pin. NORA-B2x6 modules can't be mounted inside a metal enclosure. Metal casings or plastics that include metal flakes should not be used. Metallic-based paints and lacquers should also be avoided.

3.2.4.1 Internal PCB trace antenna

For optimal operating performance, observe the following layout considerations when developing the antenna layout:

- The module shall be placed in the center of an edge of the host PCB.
- A large ground plane on the host PCB is a prerequisite for good antenna performance. A ground plane extending at least 10 mm on the three non-edge sides of the module is recommended, as shown in [Figure 6](#).
- Include a non-disruptive GND plane underneath the module with a cut out underneath the antenna, as shown in [Figure 6](#).
- Observe the antenna "keep-out" area on all layers, as shown in figures [Figure 6](#).
- NORA-B206 has six GND pads located close to the antenna, as shown in [Figure 6](#). Connect these pads to GND. Detailed dimensions of the footprint, including those related to these GND pads, can be found in the NORA-B206 series data sheet [\[2\]](#).
- To avoid degradation of the antenna characteristics, do not place physically tall or large components closer than 10 mm to the module antenna.
- To avoid any adverse impact on antenna performance, include a 10 mm clearance between the antenna and the casing. Polycarbonate (PC) and Acrylonitrile butadiene styrene (ABS) materials have less impact on antenna performance than other types of thermoplastics.
- Include plenty of stitching vias from the module ground pads to the GND plane layer. Ensure that the impedance between the module pads and ground reference is minimal.
- Connect all ground pads to the ground plane.
- Consider the end products use case and assembly to make sure that the antenna is not obstructed by any external item.

Figure 6 shows the ground plane on both sides of the module and the antenna “keep-out” area on all layers.

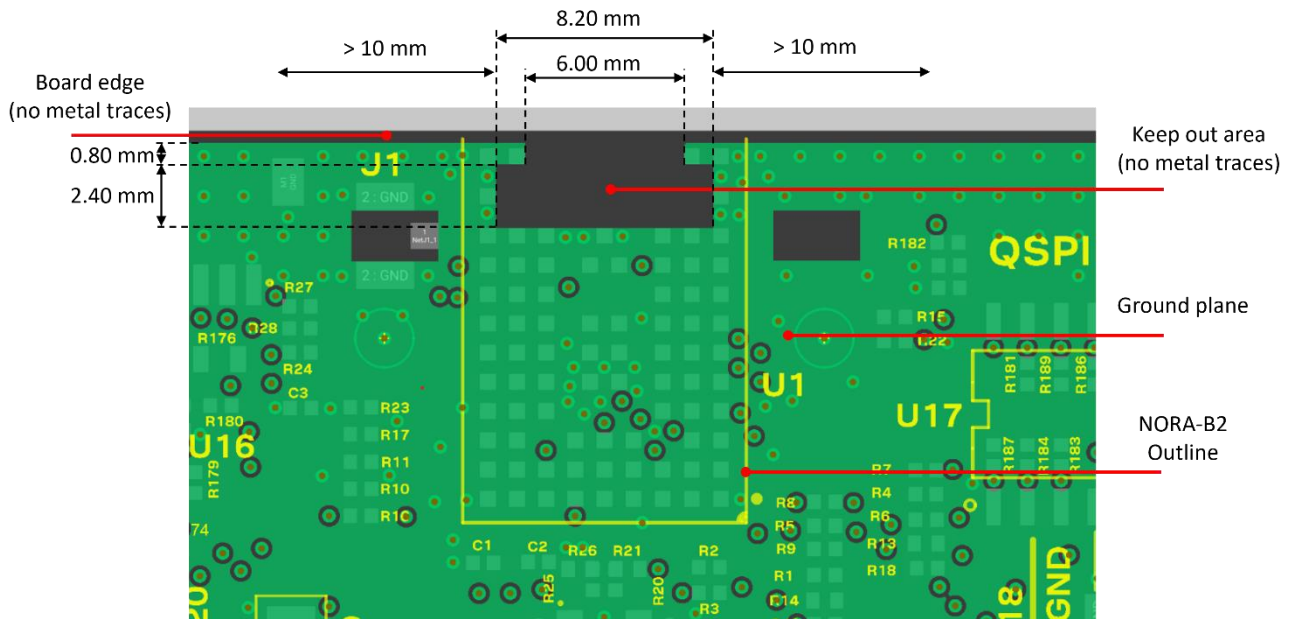


Figure 6: Extended host ground plane outside NORA-B206

3.3 General layout guidelines

This section describes the best practice for the schematic design and circuit layout of the application.

3.3.1 Considerations for schematic design and PCB floor planning

- Low frequency signals are generally not critical to the layout and designers should focus on the higher speed buses. One exception to this general rule is when high impedance traces, such as signals driven by weak pull resistors, might be affected by crosstalk. For these and similar traces, a supplementary isolation of $4w$ (four times the line width) from other buses is recommended.
- Verify which interface bus requires termination and add series resistor terminations to these buses.
- Carefully consider the placement of the module with respect to antenna position and host processor.
- Verify the controlled impedance dimensions of the selected PCB stack-up. The PCB manufacturer might be able to provide test coupons.
- Verify that the power supply design and power sequence are compliant with module specifications, as described in the module’s data sheet.

- Take particular care not to place components close to the antenna area and follow the recommendations from the antenna manufacturer to determine the safe distance between the antenna and any other part of the system. Designers should also maximize the distance between the antenna and high-frequency buses, like DDRs and related components, or consider the use of an optional metal shield to reduce the potential interference picked up by the module antenna.

3.3.2 Component placement

- Place the module such that it provides optimum RF performance. This includes short low loss antenna connections and unobstructed antenna placement. For more information about the module placement and other antenna considerations, see also [Antenna Integration](#).
- Place bypass capacitors as close as possible to the module. Prioritize the placement of capacitors with the least capacitance so that these are closest to module pads. The supply rails must be routed through the capacitors from the power supply to the supply pad on the module.
- Do not place components close to the antenna area. Follow the recommendations of the antenna manufacturer to determine distance of the antenna in relation to other parts of the system. Designers should also maximize the distance of the antenna to High-frequency busses, like DDRs and related components. Alternatively, consider an optional metal shield to reduce interferences that might otherwise be picked up by the antenna and subsequently reduce module sensitivity.

3.3.3 Layout and manufacturing

- Avoid stubs on high-speed signals which might adversely affect signal quality. Test points or component pads should be placed over the PCB trace.
- Verify the recommended maximum signal skew for differential pairs and length matching of buses.
- Minimize the routing length. Ensure that the maximum allowable length for high-speed buses is not exceeded. Longer traces generally degrade signal performance.
- For impedance matched traces, consult with your PCB manufacturer early in the project for proper stack-up definition.
- Separate the RF and digital sections of the board.
- Don't split ground layers under the module.
- Minimize the routing length. Ensure that the maximum allowable length for high-speed buses is not exceeded. Longer traces generally degrade signal performance.
- Couple all traces (including low speed or DC traces) with a reference plane (GND or power), and reference all hi-speed buses against the ground plane. If any ground reference needs to be changed, add an adequate number of GND vias in the area in which the layer is switched. This is necessary to provide a low impedance path between the two GND layers for the return current.
- Don't change the reference plane for Hi-Speed buses. If changes in the reference plane are unavoidable, add capacitors in the transition area of the reference planes. This is necessary to ensure that a low impedance return path exists through the different reference planes.
- Following the "3w rule", keep traces at a distance no less than three times that of its own width from the routing edge of the ground plane.
- For EMC purposes and the need to shield against any potential radiation, it is advisable to add GND stitching vias around the edge of the PCB. Traces on the PCB peripheral are not recommended.

3.4 Module footprint and paste mask

Figure 7 shows the recommended stencil design for the copper pad layout in NORA-B2x1.

The proposed land pattern layout complements the pin layout of the module. Both Solder Mask Defined (SMD) and Non-Solder Mask Defined (NSMD) pins can be used – with adherence to the following considerations:

- All pins should be Non-Solder Mask Defined (NSMD)
- To help with the dissipation of the heat generated by the module, GND pads must have good thermal bonding to PCB ground planes.

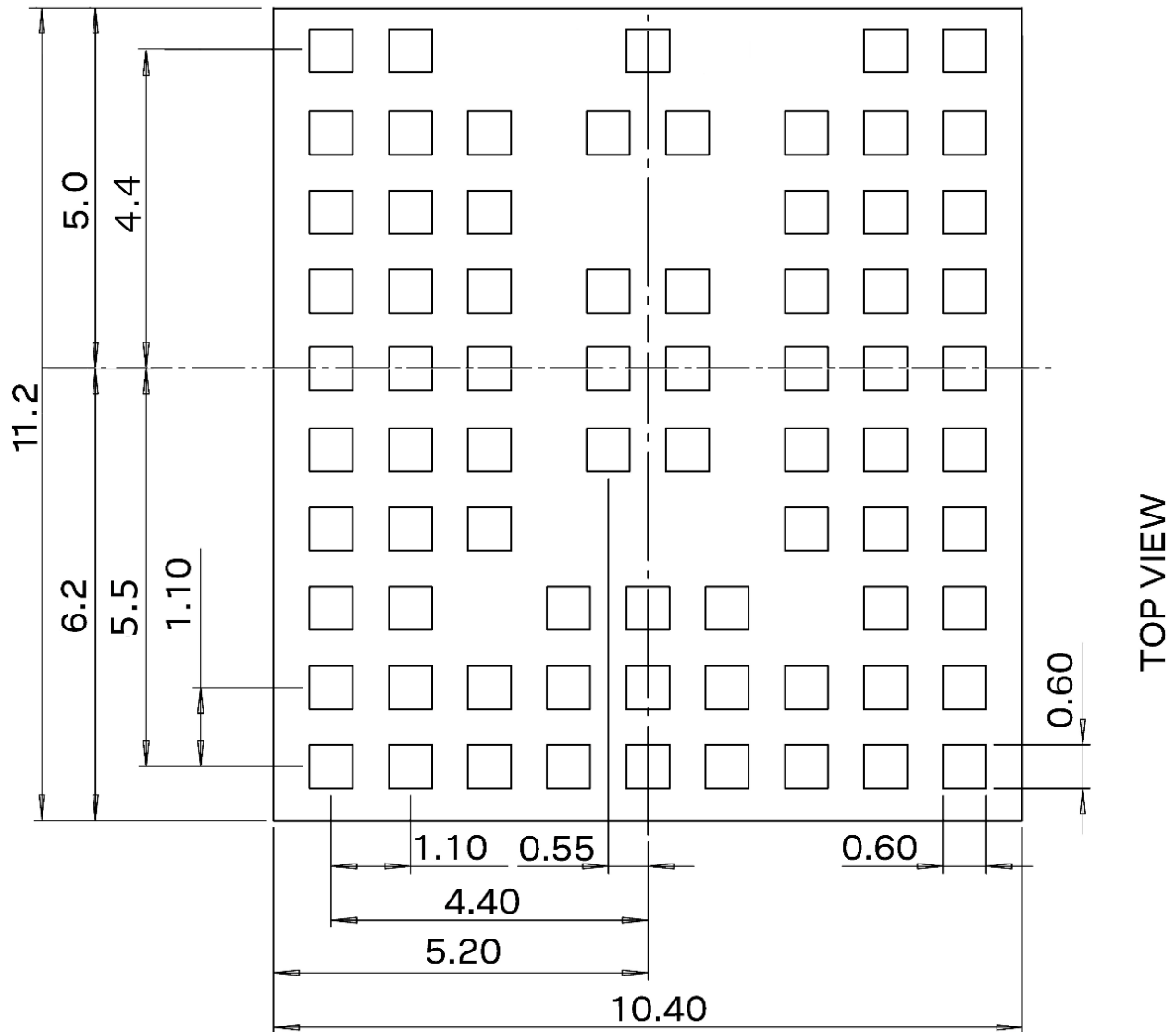
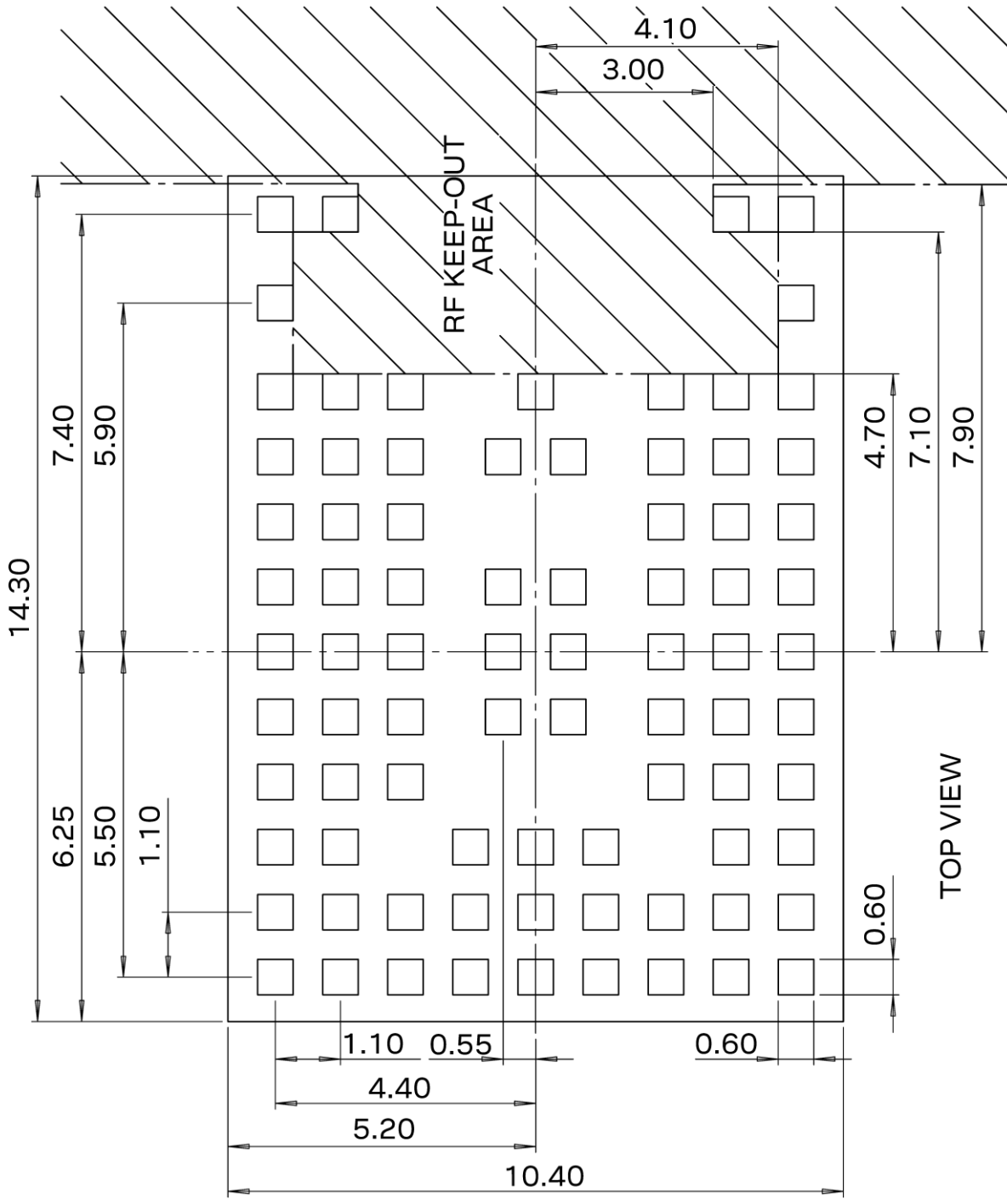


Figure 7: Recommended footprint for NORA-B2x1 (bottom view)

Figure 8 shows the recommended stencil design for the copper pad layout in NORA-B2x6.

The proposed land pattern layout complements the pin layout of the module. Both Solder Mask Defined (SMD) and Non-Solder Mask Defined (NSMD) pins can be used with adherence to the following considerations:

- All pins should be Non-Solder Mask Defined (NSMD)
- To help with the dissipation of the heat generated by the module, GND pads must have good thermal bonding to PCB ground planes.



>

Figure 8: Recommended footprint for NORA-B2x6 (bottom view)

3.5 ESD guidelines


Device immunity against Electrostatic Discharge (ESD) is a requirement for Electromagnetic Compatibility (EMC) conformance and use of the CE marking for products intended for sale in Europe. To bear the CE mark, all application products integrating u-blox modules must be conformance tested in accordance with the R&TTE Directive (99/5/EC), the EMC Directive (89/336/EEC) and the Low Voltage Directive (73/23/EEC) issued by the Commission of the European Community.

Compliance with the above directives implies conformity to the following European Norms for device ESD immunity: ESD testing standard CENELEC EN 61000-4-2 and the radio equipment standards ETSI EN 301 489-1, ETSI EN 301 489-7, ETSI EN 301 489-24, the requirements of which are summarized in [Table 6](#).

The ESD immunity test is performed at the enclosure port, defined by *ETSI EN 301 489-1* as the physical boundary through which the electromagnetic field radiates. If the device implements an integral antenna, the enclosure port is seen as all-insulating and includes conductive surfaces to house the device. If the device implements a removable antenna, the antenna port can be separated from the enclosure port. The antenna port includes the antenna element and its interconnecting cable surfaces.

Any extension of the ESD immunity test to the whole device is dependent on the device classification, as defined by *ETSI EN 301 489-1*. Applicability of ESD immunity test to the related device ports or the related interconnecting cables to auxiliary equipment, depends on the device accessible interfaces and manufacturer requirements, as defined by the *ETSI EN 301 489-1*.

Contact discharges are performed at conductive surfaces, while air discharges are performed at insulating surfaces. Indirect contact discharges are performed on the measurement setup horizontal and vertical coupling planes as defined in the *CENELEC EN 61000-4-2*.

 The terms “integral antenna”, “removable antenna”, “antenna port”, “device classification” used in the context of this guideline are defined in *ETSI EN 301 489-1*. The terms “contact discharge” and “air discharge” are defined in *CENELEC EN 61000 4-2*.

[Table 6](#) describes the ESD immunity requirements as defined by *CENELEC EN 61000-4-2*, *ETSI EN 301 489-1*, *ETSI EN 301 489-7*, *ETSI EN 301 489-24*.

Parameter	Min.	Typical	Max.	Unit	Remarks
ESD immunity. All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration			8*	kV	Indirect discharge according to IEC 61000-4-2
ESD sensitivity, tested for all pins except ANT and RSVD pins #11, #15, #33			2.0*	kV	Human body model according to JEDEC JS001

* Test pending

Table 6 : Electro-Magnetic Compatibility ESD immunity requirements

NORA-B2 is manufactured with consideration to the specific standards for minimizing the occurrence of ESD events. The highly automated process complies with the *IEC61340-5-1 (STM5.2-1999 Class M1 devices)* standard, and designers should implement proper measures to protect devices from ESD events on any pin that might be exposed to the end user.

Compliance with standard protection level specified in *the EN61000-4-2* is achieved by including ESD protection as close to any areas accessible to the end user.

3.6 Design-in checklists

3.6.1 Schematic checklist

- All module pins are properly numbered and designated in the schematic (including thermal pins).
- Power supply design complies with the specification.
- Adequate bypassing is included in front of each power pin.
- Each signal group is consistent with its own power rail supply or proper signal translation has been provided.
- Unused pins are properly terminated.
- A pi-filter is provided in front of the antenna for final matching.
- Additional RF co-location filters have been considered in the design.

3.6.2 Layout checklist

- PCB stack-up and controlled impedance traces follow the recommendations given by the PCB manufacturer.
- All pins are properly connected, and the footprint follows u-blox pin design recommendations.
- Proper clearance is provided between the RF and digital sections of the design.
- Proper isolation is provided between antennas (RF co-location, diversity, or multi-antenna design).
- Bypass capacitors have been placed close to the module.
- Controlled impedance traces are properly implemented in the layout (both RF and digital) and the recommendations provided by the PCB manufacturer have been followed.
- 50 Ω RF traces and connectors follow the rules described in [Antenna Integration](#).
- Antenna design is reviewed by the antenna manufacturer.
- Proper grounding is provided to the module for the low impedance return path.
- Reference plane skipping is minimized for high frequency busses.
- All traces and planes are routed inside the area defined by the main ground plane.
- u-blox has reviewed and approved the PCB².


² Applicable only for end-products based on u-blox reference designs

4 Open CPU software

NORA-B2 series modules are delivered without any pre-flashed software. It needs to be loaded with an application to be functional. Nordic Semiconductor provides the nRF Connect SDK that can be used for development of applications for the NORA-B2 module.

4.1 nRF Connect SDK

The nRF Connect SDK [23] is a simple-to-use Software Development Kit (SDK), which is based on the open-source Zephyr real-time operating system with Visual Studio Code used as IDE.

 At the time of writing the Zephyr board configuration for the u-blox EVK (`ubx_evknorab2`) is not yet published. For early adopters it is advised to modify the board definition for the Nordic Semiconductor Product Development Kit `nrf54115dk` to fit the NORA-B2 and the custom board developed.

4.1.1 Installation

To get started with nRF Connect SDK:

1. Install the Toolchain Manager from the nRF Connect for Desktop application [26].
2. From the Toolchain Manager, install the selected version of the nRF Connect SDK. For more information, see the nRF Connect SDK documentation [23].

4.1.2 Custom board support configuration

A board configuration that defines the module interfaces needs to be defined to use the nRF Connect SDK.

A board definition for the u-blox EVB (`ubx_evknorab2`) can be found in the u-blox open CPU GitHub repository [19]. This definition can be used as basis for any board based on NORA-B2.


4.1.3 Support – Nordic DevZone

For support on questions related to the development of software using the nRF Connect SDK, refer to the Nordic Semiconductor DevZone forum at devzone.nordicsemi.com where both public and private questions can be posted.

4.2 Load capacitance for high-frequency oscillator

NORA-B2 has an oscillator mounted internally in the module to provide the SoC with a high frequency clock signal. For this to work properly the load capacitors internally in the SoC must be configured with the right values. In the Zephyr OS configuration this can be done using a device tree configuration, as follows:

```
&hfxo {
    load-capacitors = "internal";
    load-capacitance-femtofarad = <15250>;
};
```

 This device tree node needs to be part of the board configuration for any board utilizing the NORA-B2 modules.

See also the `ubx_evknorab2` example board definition in the u-blox open CPU GitHub repository [19].

4.3 UICR registers

The chip in the NORA-B2 modules includes a set of registers called the UICR, User Information Configuration. The registers are used to hold various device data, like the serial number and other useful information, during customer production.

The following `nrfjprog` commands can be used to write, save and restore the whole memory area:

```
$ nrfjprog.exe --memwr <address> --val <4 byte value>

$ nrfjprog.exe --readuicr uicr.hex
...
$ nrfjprog.exe --program uicr.hex
```

4.4 32 kHz crystal

NORA-B2 modules are delivered without an external low frequency crystal oscillator (LFXO). To configure the software correctly for your configuration, follow the steps in the RC oscillator configuration application note *RC oscillator configuration for nRF5 open CPU modules* [24].

 NORA-B2 EVKs are delivered with an external low frequency crystal oscillator mounted.

4.5 Setting output power

Output power for Bluetooth transmissions can be configured from within the nRF Connect SDK, using the following settings:

- Statically by setting `CONFIG_BT_CTLR_TX_PWR_PLUS_4=y` in the `prj.conf` file. Replace `PLUS_4` with your desired output power.
- Dynamically by using the HCI interface. For an example of how to set TX power using the HCI interface, see the Zephyr Bluetooth sample HCI Power Control.


For more information about antenna gain and regulatory compliance, see [Antenna integration](#) and [Regulatory compliance](#).


4.6 Flashing Open CPU software

To flash NORA-B20x modules over the Serial Wire Debug (SWD) interface an external debugger must be connected to the SWD interface of the module. Third-party tools, like J-Link Commander, J-Flash, nRF Command Line Utilities or nRF Connect Programmer, are used to flash the module.

The nRF54Lxx chip in the NORA-B2 module has the debug access port protection functionality APPROTECT enabled by default, which means that for empty modules a recovery operation (`nrfjprog -recover` or `nrfutil device recover`) is needed to be able to access the debug functionality of the module. This erases all user available non-volatile memory and disables the readback protection mechanism.

For more information about the APPROTECT and related security functionality, see the *nRF54L 15, nRF54L 10 and nRF54L05 data sheet* [28].

 SEGGER J-Link BASE external debugger works with NORA-B2xx modules.

 EVK-NORA-B2xx incorporates an onboard debugger, which means that it can be flashed without an external debugger.

4.7 Radio test software

This chapter describes the various test procedures for NORA-B2, including:

- General radio testing
- Bluetooth specific testing using Direct Test Mode (DTM)
- 802.15.4 testing

These test methods involve the use of sample applications [21][20][21] provided by the NORA-B2 chipset supplier, Nordic Semiconductor, in their nRF Connect SDK [23].

The NORA-B2 module undergoes extensive certification and approval testing, but in some instances customers may find some extra testing necessary. The additional tests are typically necessary when:


- adding a country where the NORA-B2 module is not yet certified
- adding a new antenna not covered by u-blox certification

4.7.1 Using software samples

The samples used to perform the different types of radio testing must be compiled for the board they are going to run on. For this purpose, u-blox provides board files that are adapted for the u-blox evaluation board (EVB). As a starting point for your testing, use the board files archived in the u-blox open CPU GitHub repository [19].

4.7.1.1 Considerations

When testing with a u-blox evaluation board be aware that it includes a mounted 32.768 kHz crystal oscillator. If your target board doesn't have this oscillator fitted, you must recompile the application with the changed settings when testing on your target board. For more information about this, see the application note *RC oscillator configuration for nRF5 open CPU modules* [24].

 The NORA-B2 module and EVK-NORA-B2 evaluation board have different pin mappings than the evaluation boards supplied by Nordic Semiconductor. Ensure that the software you use is compiled with the correct pin mapping. For more information, see the u-blox open CPU GitHub repository [19].

4.7.1.2 Compiling samples

Compile samples using nRF Connect SDK using the correct board definition to get the UART pins correctly set up. A board definition for the u-blox EVB (`ubx_evknorab2`), which can be used as basis for the definition of any board based on NORA-B2, can be found in the u-blox Open CPU GitHub repository [19].

4.7.2 Radio test sample

The Radio test sample [21] allows the radio to be configured for transmission and reception using either modulated or constant carriers. For example, this test sample can be used to configure the radio to comply with different frequency bands (spurious emissions) and to adjust the module's output power.

4.7.2.1 Compiling the software

As the software is controlled using CLI commands over the UART interface, running the sample on the NORA-B2 module requires compiling the software with the correct pin definitions for your board.

4.7.2.2 Running the sample

This software does not use standard signaling, so regular devices like mobile phones cannot detect its signals. Instead, use another development kit running the Radio Test software as a peer device, or test with an RSSI viewer.

4.7.3 Direct Test Mode sample

The Direct Test Mode sample [20] allows the radio to be configured for transmission and reception of Bluetooth messages using different parameters. This software can be used with protocol testers that are using the DTM UART test interface as described in the *Bluetooth Core Specification* [25], volume 6, part F.

4.7.3.1 Compiling the software

As the software is controlled using CLI commands over the UART interface, running the sample on the NORA-B2 module requires compiling the software with the correct pin definitions for your board.

4.7.3.2 Running the sample

This software does not use standard signaling, so regular devices like mobile phones cannot detect the transmitted signals. Instead, use another development kit running the DTM Test software as a peer device. For testing it is convenient to drive the application using the Direct Test Mode application in *nRF Connect for desktop* [26], which provides a convenient GUI for controlling the device running the DTM sample.

4.7.4 802.15.4 PHY test tool

The 802.15.4 PHY test tool [22] performs *IEEE 802.15.4 RF Performance and PHY Certification tests* and provides information about the general performance evaluation of the integrated 802.15.4 radio.

4.7.4.1 Compiling the software

As the software is controlled using CLI commands over the UART interface, running the sample on the NORA-B2 module requires compiling the software with the correct pin definitions for your board.

4.7.4.2 Running the test tool

This test requires two development kits running the 802.15.4 test tool. For more information, see the documentation included with the 802.15.4 PHY test tool [22].

5 Handling and soldering

No natural rubbers, hygroscopic materials or materials containing asbestos are employed.

- ⚠** NORA-B2 series modules are Electrostatic Sensitive Devices that demand the observance of special handling precautions against static damage. Failure to observe these precautions can result in severe damage to the product.

5.1 ESD handling precautions

As the risk of electrostatic discharge in the RF transceivers and patch antennas of the module is of particular concern, standard ESD safety practices are prerequisite. See also [Figure 9](#).

Consider also:

- When connecting test equipment or any other electronics to the module (as a standalone or PCB-mounted device), the first point of contact must always be to local GND.
- Before mounting an antenna patch, connect the device to ground.
- When handling the RF pin, do not touch any charged capacitors. Be especially careful when handling materials like patch antennas (~10 pF), coaxial cables (~50-80 pF/m), soldering irons, or any other materials that can develop charges.
- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk of the exposed antenna being touched in an unprotected ESD work area, be sure to implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the RF pin on the receiver, be sure to use an ESD-safe soldering iron (tip).

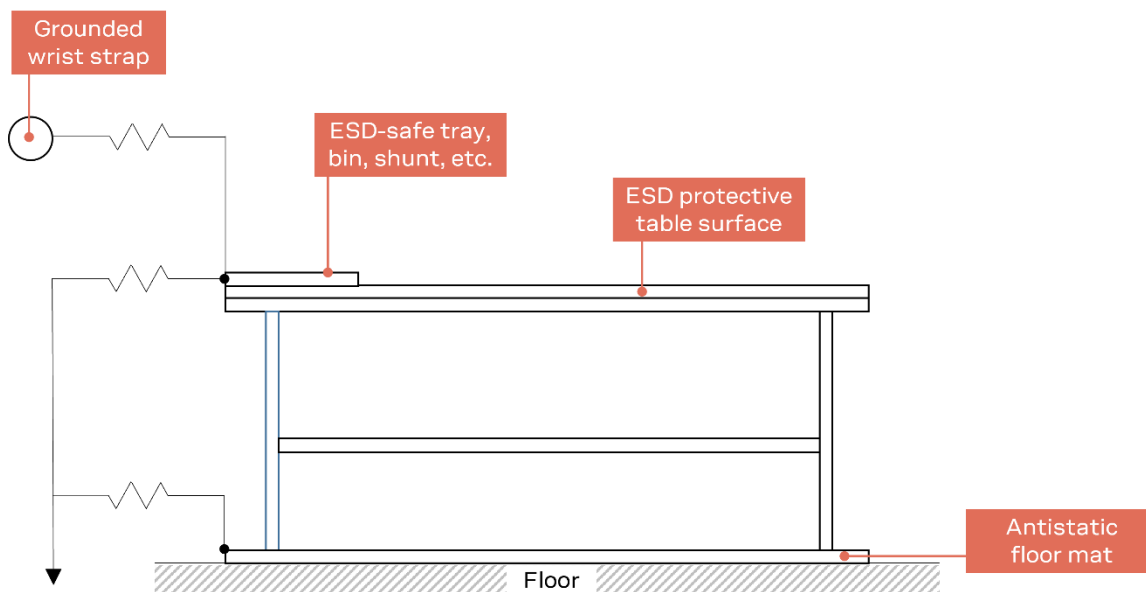


Figure 9: Standard workstation setup for safe handling of ESD-sensitive devices

5.2 Packaging, shipping, storage, and moisture preconditioning

For information pertaining to reels, tapes or trays, moisture sensitivity levels (MSL), shipment and storage, as well as drying for preconditioning, refer to the respective NORA-B2 series data sheet [\[2\]](#) and Product packaging reference guide [\[1\]](#).

5.3 Reflow soldering process

NORA-B2 series modules are surface mounted devices supplied in a Land Grid Array (LGA) package with gold-plated solder lands. The modules are manufactured in a lead-free process with lead-free soldering paste.

The thickness of solder resist between the host PCB top side and the bottom side of the module must be considered for the soldering process.

NORA-B2 modules are compatible with the industrial reflow profile for common SAC type RoHS solders. No-clean soldering paste is strongly recommended.

The reflow profile is dependent on the thermal mass over the entire area of the fully populated host PCB, the heat transfer efficiency of the oven, and the type of solder paste that is used. The optimal soldering profile that is used must be trimmed for each case depending on the specific soldering process and PCB layout.

The target values shown in [Table 7](#) are only general guidelines for a Pb-free process. For further information, see also the JEDEC J-STD-020C standard [\[6\]](#).

Process parameter		Unit	Target
Pre-heat	Ramp up rate to T_{SMIN}	K/s	3
	T_{SMIN}	°C	150
	T_{SMAX}	°C	200
	t_s (from +25 °C)	s	150
	t_s (Pre-heat)	s	60 to 120
Peak	T_L	°C	217
	t_L (time above T_L)	s	40 to 60
	T_P (absolute max)	°C	245
Cooling	Ramp-down from T_L	K/s	4
	Allowed soldering cycles	-	2

Table 7: Recommended reflow profile

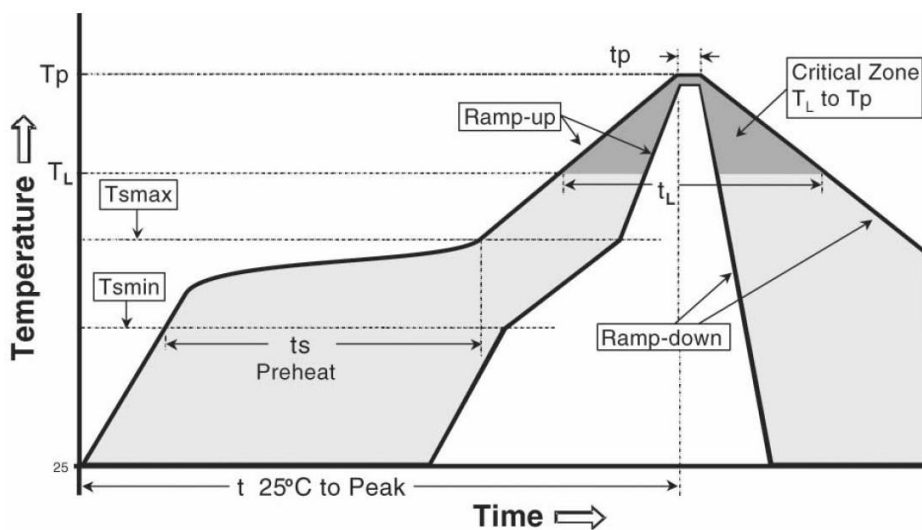



Figure 10: Reflow profile

Lower value of T_P and slower ramp down rate (2–3 °C/sec) is preferred.

5.3.1 Repeated reflow soldering

For application boards with components on both sides, a two-reflow process may be required. In such cases, NORA-B2 can be mounted in both reflow cycles. To reduce the risk of detachment due to its relatively higher weight compared to other components on the board, it is advisable to place the module on the side of the board that undergoes the final cycle. This reduces the risk of detachment due to its relatively higher weight compared to other components.

Mounting the module in an upside-down position (with the module on the underside of the board during reflow) is not recommended, as this increases the likelihood of detachment.

-  u-blox does not provide warranty coverage for damages to NORA-B2 modules caused by performing more than two total reflow soldering processes (one for mounting the module and one for mounting other components).

5.3.2 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pins. Water will also damage the sticker and the inkjet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the housing, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module and the crystal oscillators in particular.

For best results use a "no clean" soldering paste and circumvent the need for a cleaning stage after the soldering process.

5.3.3 Other notes

- Two reflow soldering processes are allowed for boards with a module soldered on it.
- Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices may require wave soldering to solder the THT components. Only a single wave-soldering process is allowed for boards populated with the modules. Miniature Wave Selective Solder processes are preferred over traditional wave soldering processes.
- Hand-soldering is not recommended.
- Rework is not recommended.
- Conformal coating can affect the performance of the module, which means that it is important to prevent the liquid from flowing into the module. The RF shields do not provide protection for the module from coating liquids with low viscosity; therefore, care is required while applying the coating. Conformal Coating of the module will void the warranty.
- Grounding metal covers: Attempts to improve grounding by soldering ground cables, wick, or other forms of metal strips directly onto the EMI covers is done so at the customer's own risk and will void the module warranty. The numerous ground pins are adequate to provide optimal immunity to interferences.
- The modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding, etc.) may damage the module. The use of ultrasonic processes during the integration of the module into an end product will void the warranty.

6 Regulatory compliance

Approvals pending.

6.1 Pre-approved antennas

Approvals pending.

This section describes the external antennas that are pre-approved for use together with NORA-B2 series modules. The currently limited list of antennas is to be extended once the scope of the module certification is decided.

Note that not all antennas and accessories are approved for use in all markets/regions.

6.1.1 Single band antennas


The following antennas are yet to be decided and may be changed without prior notice.

NORA-B206, NORA-B216, NORA-B226	
Applicable module	NORA-B2x6
Manufacturer	u-blox (Abracon license)
Gain	+2 dBi
Impedance	N/A
Size	Integrated into module
Type	PCB trace
Comment	PCB antenna on NORA-B206 and NORA-B216, and NORA.B226. This antenna is not suitable for mounting inside a metal enclosure.
Approval	FCC*, ISED*, RED*, UKCA*, MIC*, KCC*, ANATEL*, RCM*, NCC*, and ICASA*



*Approvals pending

7 Technology standards compliance

 Approvals pending.

7.1 Bluetooth SIG



® The NORA-B2 module series is qualified as a tested component according to the Bluetooth 5.4 specification (NORA-B20 series).

Product type	QDID	Listing date
NORA-B20 RF-PHY Component (Tested)	TBD	08-Mar-2021

Table 8: NORA-B2 series Bluetooth qualified design ID

The Bluetooth SIG requires the following:

- All manufacturers of products that use Bluetooth technology are required to become members of the Bluetooth SIG.
- All end-products or end-product family that utilize Bluetooth technology must be declared with the Bluetooth SIG.

For details regarding the declaration process, see the Bluetooth qualification process for nRF5 modules, application note [\[27\]](#).

7.2 Matter

End-products that incorporate the Matter protocol are required to join the [Connectivity Standards Alliance](#) and certify the end-product.

7.3 Thread

End-products that incorporate the Thread protocol are required to join the [Thread Group](#) and certify the end-product.

7.4 Zigbee

End-products that incorporate the Zigbee protocol are required to join the [Connectivity Standards Alliance](#) and certify the end-product.

7.5 USB

End-products that incorporate USB technology are required to join the [USB Implementors Forum \(USB-IF\)](#) and certify the end-product with the USB.

8 Product testing

8.1 u-blox in-line production test

As part of our focus on high quality products, u-blox maintain stringent quality controls throughout the production process. This means that all units in our manufacturing facilities are fully tested and that any identified defects are carefully analyzed to improve future production quality.

The Automatic test equipment (ATE) deployed in u-blox production lines logs all production and measurement data – from which a detailed test report for each unit can be generated. [Figure 11](#) shows the ATE typically used during u-blox production.

u-blox in-line production testing includes:

- Digital self-tests (firmware download, MAC address programming)
- Measurement of voltages and currents
- Functional tests (host interface communication)
- Digital I/O tests
- Measurement and calibration of RF characteristics in all supported bands, including RSSI calibration, frequency tuning of reference clock, calibration of transmitter power levels, etc.
- Verification of Wi-Fi and Bluetooth RF characteristics after calibration, like modulation accuracy, power levels, and spectrum, are checked to ensure that all characteristics are within tolerance when the calibration parameters are applied.



Figure 11: Automatic test equipment for module test

8.2 OEM manufacturer production test

As all u-blox products undergo thorough in-series production testing prior to delivery, OEM manufacturers do not need to repeat any firmware tests or measurements that might otherwise be necessary to confirm RF performance. Testing over analog and digital interfaces is also unnecessary during an OEM production test.

OEM manufacturer testing should ideally focus on:

- Module assembly on the device; it should be verified that:
 - Soldering and handling process did not damage the module components
 - All module pins are well soldered on device board
 - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
 - Communication with host controller can be established
 - The interfaces between module and device are working
 - Overall RF performance test of the device including antenna


In addition to this testing, OEMs can also perform other dedicated tests to check the device. For example, the measurement of module current consumption in a specified operating state can identify a short circuit if the test result deviates that from that taken against a “Golden Device”.

The standard operational module firmware and test software on the host can be used to perform functional tests (communication with the host controller, check interfaces) and perform basic RF performance testing. Special manufacturing firmware can also be used to perform more advanced RF performance tests.

8.2.1 “Go/No go” tests for integrated devices

A “Go/No go” test compares the signal quality of the Device under Test (DUT) with that of “Golden Device” in a location with a known signal quality. This test can be performed after establishing a connection with an external device.

A very simple test can be performed by just scanning for a known Bluetooth low energy device and checking that the signal level (Received Signal Strength Indicator (RSSI)) is acceptable.

 Tests of this kind may be useful as a “go/no go” test but are not appropriate for RF performance measurements.

Go/No go tests are suitable for checking communication between the host controller and the power supply. The tests can also confirm that all components on the DUT are well soldered.

A basic RF functional test of the device that includes the antenna can be performed with standard Bluetooth low energy devices configured as remote stations. In this scenario, the device containing NORA-B2 and the antennas should be arranged in a fixed position inside an RF shield box. The shielding prevents interference from other possible radio devices to ensure stable test results.

Appendix

A Glossary

Abbreviation	Definition
ABS	Acrylonitrile butadiene styrene
ADC	Analog to Digital Converter
ATE	Automatic Test Equipment
LE	(Bluetooth) Low Energy
CLI	Command Line Interface
CTS	Clear To Send
DCE	Data Circuit-terminating Equipment / Data Communication Equipment
DCX	Data/Command Signal
DDR	Dual-Data Rate
DFU	Device Firmware Update
DTE	Data Terminal Equipment
DTM	Direct Test Mode
EMC	Electro Magnetic Compatibility
EMI	Electro Magnetic Interference
ESD	Electro Static Discharge
EVB	Evaluation Board
EVK	Evaluation Kit
FCC	Federal Communications Commission
GATT	Generic ATtribute profile
GND	Ground
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
IDE	Integrated Development Environment
IEEE	Institute of Electrical and Electronics Engineers
LDO	Low Drop Out
LED	Light-Emitting Diode
LFCLK	Low Frequency, Real Time Clock
LFXO	Low Frequency, Crystal Oscillator
MAC	Media Access Control
MISO	Main Input, Sub Output
MOSI	Main Output, Sub Input
MSL	Moisture Sensitivity Level
NBU	Narrow Band Unit
NFC	Near Field Communication
NSMD	Non-Solder Mask Defined
NVM	Non-Volatile Memory
PCB	Printed Circuit Board
PIFA	Planar Inverted-F Antenna
PC	Polycarbonate
QDEC	Quadrature Decoder
QSPI	Quad Serial Peripheral Interface

Abbreviation	Definition
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RSSI	Received Signal Strength Indicator
RTC	Real Time Clock
RTS	Request to Send
RXD	Receive Data
SCL	Signal Clock
SDL	Specification and Description Language
SMA	SubMiniature version A
SMD	Solder Mask Defined
SMPS	Switching Mode Power Supply
SMT	Surface-Mount Technology
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
Thread	Networking protocol for Internet of Things (IoT) "smart" home automation devices to communicate on a local wireless mesh network
THT	Through-Hole Technology
TWI	Two-Wire Interface
TXD	Transmit Data
UART	Universal Asynchronous Receiver/Transmitter
UICR	User Information Configuration Registers
USB	Universal Serial Bus
VCC	IC power-supply pin
VSWR	Voltage Standing Wave Ratio
Zigbee	Open standard protocol, full-stack solution for most large smart home ecosystem providers


Table 9: Explanation of the abbreviations and terms used

B Antenna reference designs

This information is pending.

Related documents

- [1] Packaging information reference, [UBX-20027119](#)
- [2] NORA-B2 series data sheet, [UBXDOC-1023859458-38975](#)
- [3] NORA-B2 series product summary,
- [4] Nordic nRF54L15 data sheet,
https://docs.nordicsemi.com/bundle/ps_nrf54L15/page/keyfeatures_html5.html
- [5] Nordic nRF54L15 Reference Manual,
- [6] EVK-NORA-B2 user guide,
- [7] JEDEC J-STD-020C - Moisture/Reflow Sensitivity Classification for Non Hermetic Solid State Surface Mount Devices
- [8] IEC EN 61000-4-2 - Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test
- [9] ETSI EN 301 489-1 - Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements
- [10] IEC61340-5-1 - Protection of electronic devices from electrostatic phenomena – General requirements
- [11] ETSI: Audio/video, information, and communication technology equipment - Part 1: Safety requirements, [IEC 62368-1:2018](#)
- [12] JESD51 – Overview of methodology for thermal testing of single semiconductor devices
- [13] NORA-B2 EU Declaration of conformity (EU DoC),
- [14] NORA-B2 UKCA Declaration of conformity (UKCA DoC),
- [15] Tag-Connect pad connector - <http://www.tag-connect.com/TC2030-CTX>
- [16] Guidance on software or network configuration of Non-SDR devices, [OET KDB 594280 D01](#)
- [17] Software security requirements for U-NII devices, [OET KDB 594280 D02](#)
- [18] Guidance for modular transmitter instruction manuals and TCB certification application reviews, [KDB 996369 D03](#)
- [19] u-blox short range open CPU repository, <https://github.com/u-blox/u-blox-sho-OpenCPU>
- [20] Documentation for Direct Test Mode sample, https://github.com/nrfconnect/sdk-nrf/tree/main/samples/bluetooth/direct_test_mode
- [21] Documentation for Radio test sample, https://github.com/nrfconnect/sdk-nrf/tree/main/samples/peripheral/radio_test
- [22] Documentation for 802.15.4 PHY test tool, https://github.com/nrfconnect/sdk-nrf/tree/main/samples/peripheral/802154_phy_test
- [23] nRF Connect SDK, <https://www.nordicsemi.com/Products/Development-software/nRF-Connect-SDK>
- [24] RC oscillator configuration for nRF5 open CPU modules, [UBX-20009242](#)
- [25] Bluetooth Core Specification, <https://www.bluetooth.com/specifications/specs>
- [26] nRF Connect for Desktop, <https://www.nordicsemi.com/Products/Development-tools/nRF-Connect-for-Desktop>
- [27] Bluetooth® qualification process – nRF Connect SDK - Application note, [UBX-21040374](#)
- [28] nRF54L15 documentation, <https://docs.nordicsemi.com/category/nRF54L15-category>

 For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R1	05-Jul-2024	Iber, mape	Initial version
R2	19-Feb-2025	Iber, mape	Deleted Medium and Normal voltage mode from Power supply section. Revised Product overview and Module integration chapters and included changes to Open CPU software and Radio test software sections with other miscellaneous revisions added throughout. Added Repeated reflow soldering section.

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