swissbit®

Swissbit Flash Products

Reliability & Data Integrity

Managing
Read Disturb Effects
Data Retention
Endurance

White Paper

made in germany

1 Overview

1.1 NAND Flash organization

NAND Flash chips are organized in Pages (2...16kB+spare) and Blocks (typically 64 pages). A page can be programmed once or up to four times, but only a full block can be erased at the same time.

1.2 Program and Erase operation → Endurance limitation

During program and erase operation the electrons are "pressed" (tunneled) through an insulator into or out of the memory cell by applying a relatively large voltage. Each of these program and erase operations causes a slight damage to the insulator which gradually shortens the data retention of the cell. The Error Correction Code (ECC) capability implemented into the controller is able to correct a given number of bit errors. The typical number of program erase cycles for the different NAND Flash Technologies are:

Flash Technology	Description	bits per cell	Endurance (PE cycles)	reads initially	reads at life end
SLC	Single level cell	1	100'000	100'000	10'000
EM–MLC	Endurance Managed MLC	2	Up to 30'000	100'000	10'000
MLC	Multi level cell	2	Up to 3'000	100'000	10'000
TLC	Triple level cell	3	<1'000		

1.3 Read operation → Read disturb limitation

In a read operation, a small voltage has to be applied, not only to the page that is actually read but also the surrounding pages in the same block. This voltage does not damage the insulator. However, depending on the state of the insulation layers in the surrounding pages in the block, electrons could be injected into them, potentially changing their charge levels. If an application reads a file or file structure (directory, FAT, ...) very often the neighbor sectors can be soft–programmed and the number of bit errors gradually increase to a level that the ECC cannot correct any more. So once the user tries to read the data it will appear as "corrupted".
Typically, the specified read disturb value of a flash cell is 100'000 read commands per block at the initial stage and 10'000 read command the Endurance life end.
Regular write operations help limiting read disturb effects as the wear leveling algorithm that is commonly implemented into NAND Flash Storage devices moves the data around internally and with that automatically corrects bit errors if required.

2 Read Disturb management

To prevent read disturb errors many Swissbit products include an active "Read Disturb Management" (RDM) where the card controller counts the number of read operations for each block. If a specific block reaches a pre–defined threshold value the controller refreshes the data by moving it into a new block and correcting the data using the ECC.

3 Other Methods to increase data retention and endurance

Swissbit memory products have different mechanisms to increase the data retention in operation. The actually implemented mechanisms vary by product

1) **Wear leveling**: The device counts the erases operations for each block. If the erase counter of a block is much larger than another block, both blocks are exchanged. This guarantees that all blocks in the Flash device are erased nearly equally.

2) **Error correction code (ECC)**: The Swissbit Flash devices are capable of correcting 40 corrupted bits in 2 adjacent sectors.

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3) **Read retry**: If the data cannot be corrected by the ECC, the controller retries reading the data using different read voltage thresholds. This can allow reconstructing the data in cells that are charged incorrectly, either because the electrons escaped the flash cells (retention issue) or accidentally injected (read disturb issue)

4) **Auto Read Refresh:** The controller reads the entire data stored in the device from time to time and compares the number of bit error against an ECC threshold. If the number of bit errors is above the threshold, the affected data is refreshed.

5) **ECC Monitoring:** The controller monitors the bit error levels in each read operation; once that reaches a preset threshold value, the controller automatically performs data refresh to "restore" the correct charge levels in the cell.

6) **EarlyRetirement**: EarlyRetirement works by moving the static data to a healthy block before the previously used block becomes completely incapable of holding charges. Once the charge loss error level exceeds a given threshold value (higher the threshold used for ECC Monitoring), the controller automatically moves its data to another block. In addition, the original block is then marked as a bad block, which prevents further use, and enters the state of "EarlyRetirement."

7) **Data Scrambling**: The controller stores the data scrambled to the flash, i.e. combined with pseudo random data. This guarantees that the numbers of "0"s and "1"s are about the same in each physical sector,. Data Scrambling balances the write current over the entire flash page, regardless of how the data was received from the host.

8) **Overprovisioning:** Some devices keep a certain percentage of the physically available Flash as some kind of cache, so the storage volume available to the user is slightly lower. Overprovisioning significantly improves random write performance and Write Amplification Factor (WAF), which increases endurance, especially once the device has been fully written several times.

9) **TRIM:** The TRIM command is supported in recent operating systems (from Windows 7) and some new SSD Models. . With this command the operating system can inform the device which data in the file system is no longer in use (e.g. deleted file). The SSD can then ignore this data when performing internal processes such as wear leveling which increases performance and endurance.

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5 Document History

Table 1: Document Revision History

Date	Revision	Details
17-February-2014	0.20	First DRAFT
17-April-2014	1.00	Release Revision

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