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CCM PFC Boost Converter Design

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DN 2013-01

Subjects: CCM PFC Boost Converter Design

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CCM PFC Boost Converter Design

Table of contents

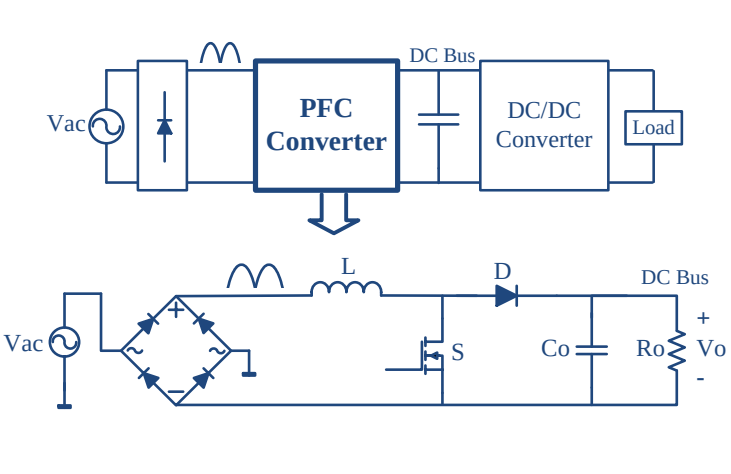
CCM PFC Boost Converter Design

1 Introduction

Power Factor Correction (PFC) shapes the input current of the power supply to be in synchronization with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as would an equivalent resistor, with no added input current harmonics. This document is intended to discuss the topology and operational mode for high power PFC applications (>300W), and provide detailed design equations with examples.

2 Boost topology

Although active PFC can be achieved by any basic topology, the boost converter (Figure 2.1) is the most popular topology used in PFC applications, for the following reasons: The line voltage varies from zero to some peak value typically 375V, hence; a step up converter is needed to output a dc bus voltage of 380V or more. For that reason the buck converter is eliminated, and the buck-boost converter has high switch voltage stress (Vin+Vo). Moreover, the boost converter has the filter inductor on the input side, which provides a smooth continuous input current waveform as opposed to the discontinuous input current of a buck or buck-boost topology. This continuous input current is much easier to filer, which is a major advantage because any additional filtering that is needed on the input side of the converter adds cost and reduces the power factor due to capacitive loading of the line.



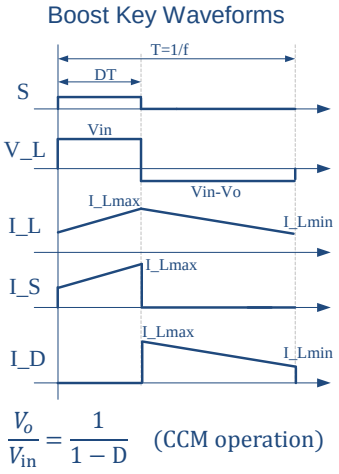


Figure 2.1

3 PFC Modes of Operation

The boost converter can operate in three modes: continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CrCM). Fig. 2 shows modeled waveforms to illustrate the inductor and input currents in the three operating modes, for the same exact voltage and power conditions.

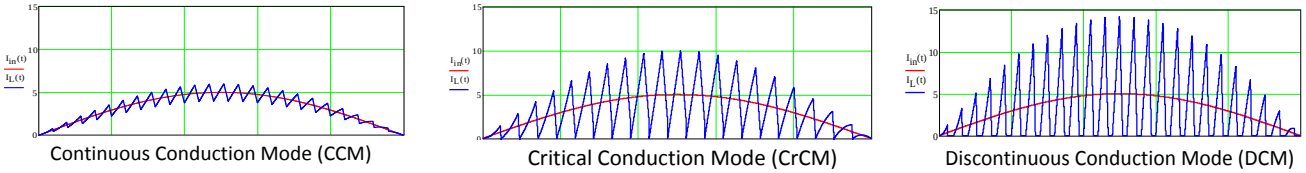


Figure 3.1

Although DCM operation seems simpler than CrCM, since it may operate in constant frequency operation, DCM has the disadvantage that it has the highest peak current compared to CCM and CrCM, but with no performance advantage compared to CrCM, and one potential disadvantage. For that reason, CrCM is a more common practice than DCM, therefore, this document will exclude the DCM mode.

CrCM may be considered a special case of CCM, where operation is controlled to stay at the boundary between CCM and DCM. CrCM usually uses constant on-time control; as the line voltage is changing across the 60Hz line cycle, the reset time for the boost inductor varies, and the operating frequency will change as well in order while maintaining boundary mode operation. CrCM dedicated controllers sense the inductor current zero crossing in order to trigger the start of the next switching cycle. When carefully designed, the boost rectifier diode for the CrCM PFC is selected not to be ultra-fast, but of medium fast speed, so that the inductor current not only completely resets to zero but may switch slightly negative. This energy stored in the CrCM boost inductor will “Flyback” to ground, achieving ZVS turn-on for the boost MOSFET under most conditions, particularly at input voltage above 200V, when this will not usually occur for a 400V nominal bulk bus system.

The current ripple (or the peak current) in CrCM is twice the average value, which greatly increases the RMS currents and turn off current. But since every switching cycle starts at zero current, and usually with ZVS operation, turn on loss is usually eliminated. Also, since the boost rectifier diode turns off at zero current as well, reverse recovery losses from Q_{rr} and noise from switching at high I_{rrm} in the boost diode are eliminated too, another major advantage of CrCM mode. Still, on the balance, the high input ripple current and it’s impact on the input EMI filter tends to eliminate CrCM mode for high power designs unless interleaved stages are used to reduce the input HF current ripple. A high efficiency design can be realized that way, but at substantially higher cost. That discussion is beyond the scope of this Design Note.

CCM PFC Boost Converter Design

The power stage equations and transfer functions for CrCM are the same as CCM. The main differences relate to the current ripple profile and switching frequency, which affects RMS and switching power losses and filter design.

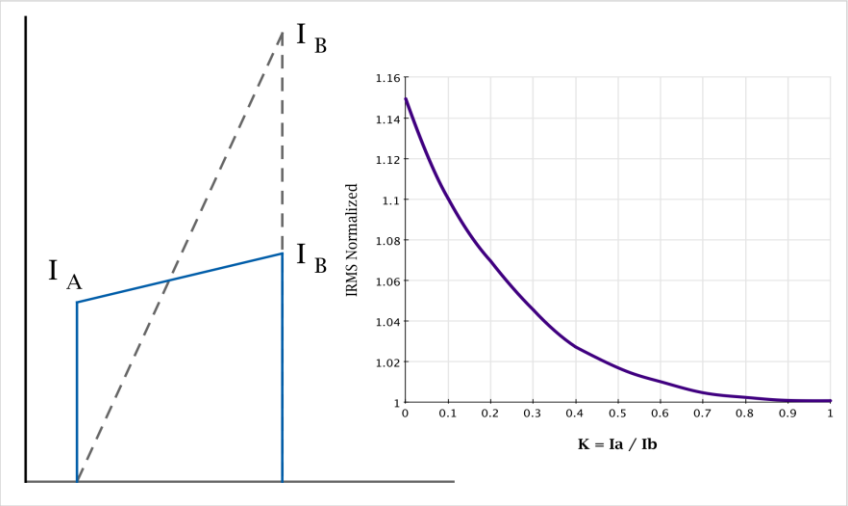


Figure 3.2 IRMS Normalized by I_A/I_B ratio in relation to current waveshape

CCM operation requires a larger filter inductor compared to CrCM. While the main design concerns for a CrCM inductor are low HF core loss, low HF winding loss, and stable value over the operating range (the inductor is essentially part of the timing circuit), the CCM mode inductor takes a different approach. For the CCM mode PFC, the full load inductor current ripple is typically designed to be 20-40% of the average input current. This has several advantages:

(1) Peak current is lower, and the RMS current factor with a trapezoidal waveform is reduced compared to a triangular waveform, reducing conduction losses (Fig 3.2).
(2) Turn off losses are lower due to switch off at much lower maximum current.
(3) The HF ripple current to be smoothed by the EMI filter is much lower in amplitude.

On the other side, CCM encounters turn on losses with the MOSFET, which can be exacerbated by the boost rectifier commutation recovery loss due to Q_{rr}. For this reason, ultra-fast recovery diodes or silicon carbide schottky diodes with no charge Q_{rr} are needed for CCM mode.

In conclusion, we can say that for low power applications, the CrCM boost has an advantage in losses and power density. This advantage may extend to medium power ranges, however at some medium power level the low filtering and the high peak current starts to become severe disadvantages. At this point the CCM boost starts being a better choice for high power applications.

According to the above, and since this document is intended to support high power PFC applications, the following are detailed design discussions and design examples for a CCM PFC boost converter.

4 CCM PFC Boost Design Equations

The following are design equations for the CCM operated boost, with a design example integrated to further clarify the usage of all equations. The boost converter encounters the maximum current stress and power losses at the minimum line voltage condition ($V_{ac.min}$); hence, all design equations and power losses will be calculated using the low line voltage condition.

Table 1 Specifications

Input voltage	85-265 VAC 60Hz
Output voltage	390V
Maximum power steady state	400W
Switching frequency	100kHz
Inductor current ripple	30%
Output voltage ripple (2x line frequency)	10 Vp-p
Hold-up time	16.6ms @ $V_{O.min}$=350V

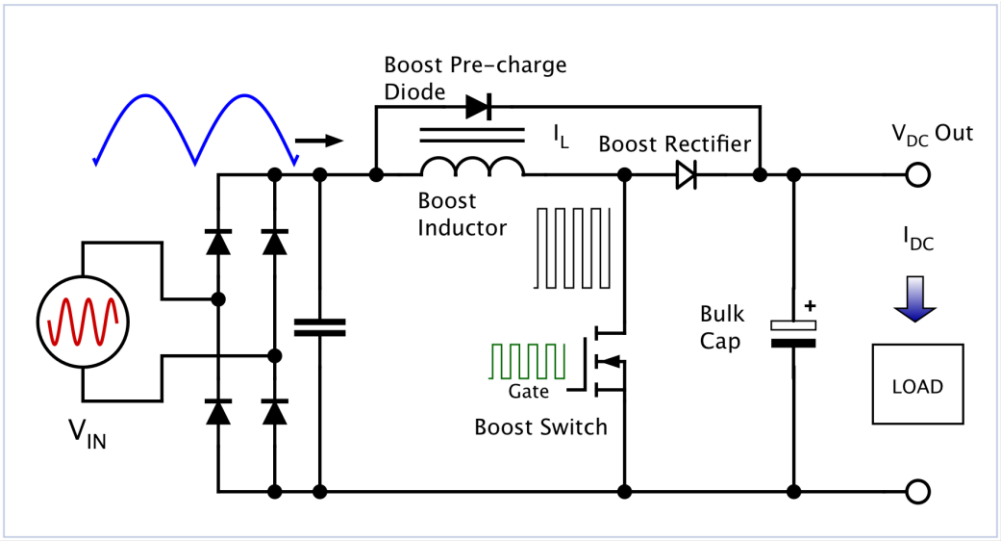


Figure 4.1 Block Schematic for boost power stage with input rectifier

Filter Inductor

The filter inductor value and its peak current are determined based on the specified maximum inductor current ripple.

$$L = \frac{1}{\%Ripple} \cdot \frac{V_{ac.min}{}^2}{P_o}\left(1 - \frac{\sqrt{2}\cdot V_{ac.\min}}{V_o}\right) \cdot T \qquad (1)$$

$$= \frac{1}{0.3} \cdot \frac{85^2}{400}\left(1 - \frac{\sqrt{2}\cdot 85}{390}\right) \cdot \frac{1}{100\cdot 10^3} = 416.5\ \mu H$$

CCM PFC Boost Converter Design

$$I_{L.pk} = \frac{\sqrt{2}\cdot P_o}{V_{ac.min}} \cdot \left(1 + \frac{\%Ripple}{2}\right) \quad (2)$$

$$= \frac{\sqrt{2}\cdot 400}{85} \cdot \left(1 + \frac{0.3}{2}\right) = 7.7\ A$$

→ Inductor saturation current, rectifier bridge, MOSFET and boost diode, must all be rated at > 7.5A . One practical design would suggest 12A current ratings.

$$I_{L.rms} = \frac{P_o}{V_{ac.min}} \quad (3)$$

$$P_{L.cond} = {I_{L.rms}}^2 \cdot DCR \quad (4)$$

$$= \left(\frac{390}{85}\right)^2 \cdot DCR = 22.1 \cdot DCR \quad Watt$$

Off the shelf inductors are available and usable for a first pass design, typically with single layer windings and a permeability droop of 30% or less [ ].

In some circumstances it may be desirable to further optimize the inductor configuration, in order to meet requirements for high power factor over a wide line and input current range, and to optimize the inductor size. Many of the popular PFC controllers use what is known as single cycle current loop control, which can provide very good performance provided that the inductor remains in CCM mode operation. At low-line this is no problem, but for operation in the high-line band (176VAC to 265VAC), the operating current will be much lower. If an inductor is used with a nominal “stable” value of inductance, what works well at low-line results in DCM mode operation for a significant part of the load range at high-line, and poorer power factor and higher EMI than necessary.

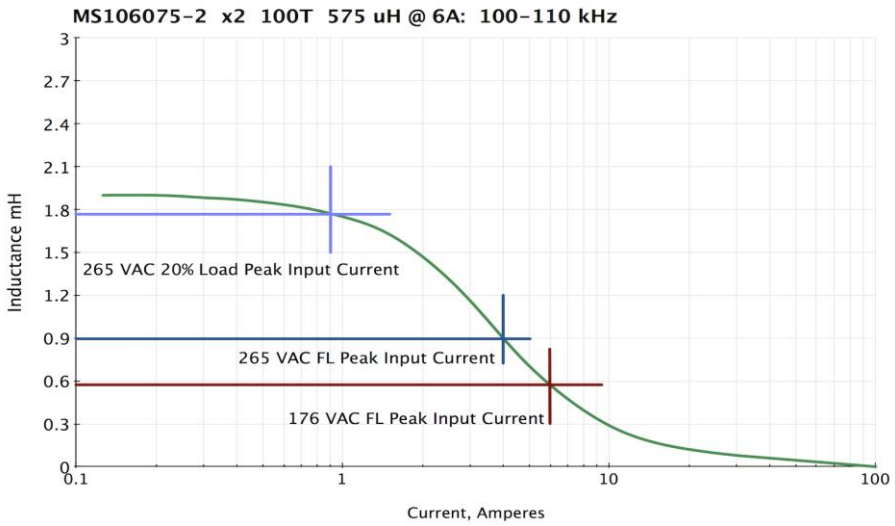


Figure 4.2 Swinging Boost Inductor example optimized for CMM mode operation over wide range

A swinging choke design can address this, by using a medium permeability core (75-125µ) of core types such as Arnold/Micrometals Sendust and Magnetics Inc. Kool Mu, of the right energy capability and designing for full load permeability droop by 75-80%, so that with lighter load the inductance swings up. The full details of this technique are beyond the scope of this design note, but it can be facilitated with available design tools from core manufacturers [2]. An example of this with operating current points referenced key line voltage points in one design example is shown in Figure 4.2.

Rectifier Bridge

The bridge total power loss is calculated using the average input current flowing through two of the bridge rectifying diodes.

$$P_{bridge} = \frac{4\cdot\sqrt{2}}{\pi}\cdot\frac{P_o}{V_{ac.min}}\cdot V_{f.bridge} \quad (5)$$

$$= \frac{4\cdot\sqrt{2}}{\pi}\cdot\frac{390}{85}\cdot V_{f.bridge} = 8.3\cdot V_{f.bridge} \quad Watt$$

Recommendation: GBJ1006-BP. Using a higher rated current bridge can reduce the forward V_F, lowering the total power dissipation at a small incremental cost. This is often a sound strategy, as with modern components, the bridge rectifier usually has the highest total semiconductor loss for the PFC stage.

MOSFET

In order to select the the optimum MOSFET, one must understand the MOSFET requirements in a CCM boost converter. High voltage MOSFETS have several families based on different technologies, which each target a specific application, topology or operation. For a boost converter, the following are some major MOSFET selection considerations:

- Low FOMs - R_{on}*Q_g and R_{on}*E_{oss}
- Fast Turn-on/off switching, gate plateau near middle of gate drive range (which balances turn-on and turn-off losses)
- Low Output capacitance C_{oss} for low switching energy, to increase light load efficiency- this relates to the R_{on}*E_{oss} metric.
- Switching and conduction losses must be balanced for minimum total loss - this is typically optimized at the low line condition (if best thermals area desired), where worse case losses and temperature rise occur. In other cases, it may be desired to optimize efficiency at a mid load condition, and ensure that the thermal design is adequate for the worst case low-line dissipation. This varies with overall system targets.
- VDS rating to handle spikes/overshoots
- Low thermal resistance $R_{thJC.}$ Package selection must consider the resulting total thermal resistance from junction to ambient, and the worst case surge dissipation- this is typically under low-line cycle skip and recovery into highline while ramping the bulk voltage back up.
- Body diode speed and reverse recovery charge are not important, since body diode never conducts in a boost converter.

CCM PFC Boost Converter Design

The recommended CoolMOS™ MOSFET series for boost applications are the CP series and the C6/E6/P6 series. CP CoolMOS™ provides fastest switching (Figure 4.3), hence, best performance, but requires careful design in terms of gate driving circuit and PCB layout [3]. The C6/E6 series provides a distinct cost advantage, with easier design, but less performance compared to CP series. The new (in 2013) P6 series approaches CP performance closely at a better price point, and is recommended for new designs that are cost sensitive. [6]

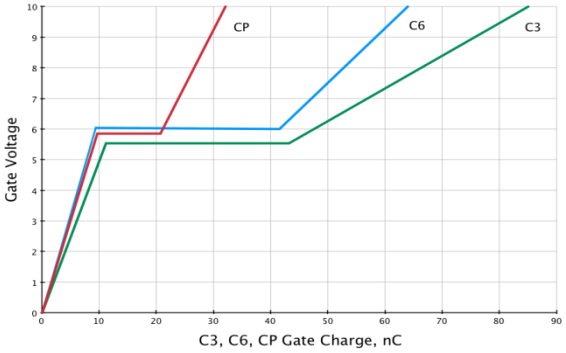


Figure 4.3

According to the aforementioned MOSFET selection criteria and to the specification listed in Table 1, the **IPW60R125CP** is selected, and its parameters will be used for the following calculations.

The MOSFET RMS current across the 60Hz line cycle can be calculated by the following equation; consequently the MOSFET conduction loss is obtained.

$$I_{S.rms} = \frac{P_o}{V_{ac.min}} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot V_{ac.min}}{3 \cdot \pi \cdot V_o}} \tag{6}$$

$$= \frac{400}{85} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot 85}{3 \cdot \pi \cdot 390}} = 4.04\ A$$

$$P_{S.cond} = {I_{S.rms}}^2 \cdot R_{on(100℃)} \tag{7}$$

$$= 4.04^2 \cdot 0.2 = 3.26\ W$$

For switching losses calculation, the average input current can be used to estimate losses over the line cycle. The average input current is given as:

$$I_{L.avg} = \frac{P_o}{V_{ac.min}} \cdot \frac{2 \cdot \sqrt{2}}{\pi} \tag{8}$$

$$= \frac{400}{85} \cdot \frac{2 \cdot \sqrt{2}}{\pi} = 4.2\ A$$

Turn-on time and loss:

$$t_{on} = Q_{gs} \cdot \frac{V_{pl} - V_{th}}{V_{pl}} \cdot \frac{2 \cdot R_g}{2 \cdot V_g - V_{pl} - V_{th}} + Q_{gd} \cdot \frac{R_g}{V_g - V_{pl}} \tag{9}$$

$$= 12 \cdot 10^{-9} \cdot \frac{5-3}{V_{pl}} \cdot \frac{2 \cdot 3}{2 \cdot 12 - 5 - 3} + 18 \cdot 10^{-9} \cdot \frac{3}{12-5} = 9.5 \cdot 10^{-9}\ s$$

$$P_{S.on} = 0.5 \cdot I_{L.avg} \cdot V_o \cdot t_{on} \cdot f \tag{10}$$

$$= 0.5 \cdot 4.2 \cdot 390 \cdot 9.5 \cdot 10^{-9} \cdot 100 \cdot 10^3 = 0.79\ \mathrm{W}$$

Turn-off time and loss:

$$t_{off} = Q_{gd} \cdot \frac{R_g}{V_{pl}} + Q_{gs} \cdot \frac{V_{pl}-V_{th}}{V_{pl}} \cdot \frac{2 \cdot R_g}{V_{pl}+V_{th}} \quad (11)$$
$$= 18 \cdot 10^{-9} \cdot \frac{3}{5} + 12 \cdot 10^{-9} \cdot \frac{5-3}{5} \cdot \frac{2 \cdot 3}{5+3} = 14.4 \cdot 10^{-9}\, s$$

$$P_{S.off} = 0.5 \cdot I_{L.avg} \cdot V_o \cdot t_{off} \cdot f \quad (12)$$
$$= 0.5 \cdot 4.2 \cdot 390 \cdot 14.4 \cdot 10^{-9} \cdot 100 \cdot 10^3 = 1.19\ \text{W}$$

This is the “classic” format for calculating turn-off time and loss; due to the high Q_{oss} of SJ MOSFETs, the C_{oss} acts like a nonlinear capacitive snubber, and actual turn-off losses with fast switching can be up to 50% lower than calculated. The current flow through the drain during turn-off under these conditions is non-dissipative capacitive current, and with fast drive, the channel may be completely turned off by the onset of drain voltage rise.

Output capacitance C_{oss} switching loss:

$$P_{S.oss} = E_{oss} \cdot f \quad (13)$$
$$= 10 \cdot 10^{-6} \cdot 100 \cdot 10^3 = 1\ \text{W}$$

Gate drive loss:

$$P_{S.gate} = V_g \cdot Q_g \cdot f \quad (14)$$
$$= 12 \cdot 53 \cdot 10^{-9} \cdot 100 \cdot 10^3 = 0.064\ \text{W}$$

$\therefore$ MOSFET total loss $= 6.3$ W

Boost Diode

Selection of the boost diode is a major design decision in CCM boost, since the diode is hard commutated at a high current, and reverse recovery can cause significant power loss, noise and current spikes. Reverse recovery can be a bottle neck for high switching frequency and high power density power supplies. Additionally, at low line, the available diode conduction duty cycle is quite low, and the forward current quite high in proportion to the average current. For that reason, the first criteria for selecting a diode in CCM boost are fast recovery with low reverse recovery charge, followed by V_F operating at high forward current.

CCM PFC Boost Converter Design

Since Silicon Carbide (SiC) Schottky diodes have capacitive charge (Q_c) rather than reverse recovery (Q_{rr}), their switching loss and recovery time are much lower compared to Silicon Ultrafast diode, and will show an enhanced performance. Moreover, SiC diodes allow higher switching frequency designs, hence, higher power density converters.

The capacitive charge for SiC diodes are not only low, but also independent on di/dt, current level, and temperature; where Si diodes have strong dependency on these conditions, as shown in Figure 4.3.

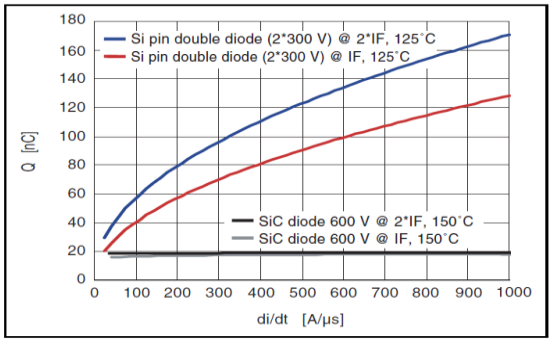


Figure 4.3

The newer generations of SiC diodes are not just Schottky devices, but are merged structure diodes known as MPS diodes - Merged PN/Schottky (Figure 4.4). They combine the relatively low V_F and capacitive charge characteristics of Schottky diodes with the high peak current capability of PN diodes, while avoiding the high junction voltage penalty (typically 2.5-3V at room temperature) of a pure PN wide bandgap diode. [4]

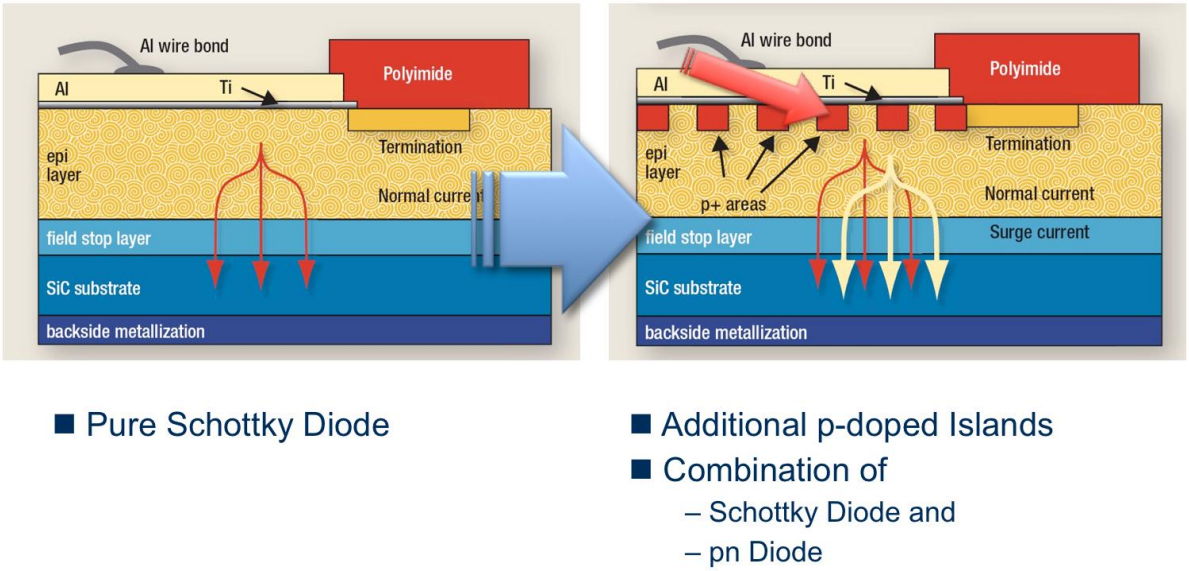


Figure 4.4 : Schottky and Merged PN/Schottky compared

The recommended diode for CCM boost applications is the 650V thinQ SiC Generation 5 diodes.

SiC G5 diodes include Infineon's leading edge technologies, such as diffusion soldering process and wafer thinning technology. The result is a new family of products showing improved efficiency over all load conditions, coming from both the improved thermal characteristics and a improved figure of merit (Q_c x V_F) [5].

With the high surge current capability of the MPS diode, there is some latitude for selection of the boost diode- a simple rule of thumb that works well for a wide input range PFC for good cost/performance tradeoffs is 1A diode rating for 80W of output power. For high-line range only applications, or high-line applications with de-rated output power at low-line conditions, this may be adjusted to as much as 150W per 1A of diode rating. In that case, for example, a 600W application in the 176 VAC to 255 VAC range will only "need" 4A. But, with the improved Q_c x V_F figure of merit, higher efficiency may be achieved by up to doubling the ID rating of the diode, especially for low-line applications where the input current is quite high with a short duty cycle. The higher rated diode will have a much lower V_F at the actual operating current, reducing conduction losses. The lower Q_c means there is no sacrifice of mid range or low range efficiency from using the larger SiC diode.

Note that even when using the MPS type SiC diode, it is still preferred to use a bulk pre-charge diode as shown earlier in Figure 4.1. This is a low frequency standard diode with high I^2t rating to support pre-charging the bulk capacitor to the peak of the AC line voltage; this is a high initial surge current stress (which should be limited by a series NTC) that is best avoided for the HF boost rectifier diode.

According to the aforementioned diode selection discussion and to the specification listed in Table 1, SiC diode **IDH12G65C5** is selected, and its parameters will be used for the following calculations.

The boost diode carries an average current equal to the output current.

$$I_{D.avg} = \frac{P_o}{V_o} \tag{15}$$

$$= \frac{400}{390} = 1.03\ A \tag{16}$$

Due to current waveforms and duty cycle, the RMS value can approach 15% higher under worst case low line conditions, but this requires a much more complex calculation to assess; a simpler form will get you in the ball park.

Diode conduction loss approximation:

$$P_{D.cond} = I_{D.avg} \cdot V_{f.diode} \tag{17}$$

$$= 1.03 \cdot 1.5 = 1.5\ W$$

Diode switching loss, which is carried by the boost MOSFET:

$$P_{D.swith} = 0.5 \cdot V_o \cdot Q_C \cdot f \tag{18}$$

$$= 0.5 \cdot 390 \cdot 18 \cdot 10^{-9} \cdot 100 \cdot 10^3 = 0.35\ \text{W}$$

$\therefore$ Diode total loss $= 1.9$ W

CCM PFC Boost Converter Design

Output Capacitor

The output capacitor is sized to meet the hold-up time and voltage ripple requirements, the capacitor is selected to have the larger value of the two equations below.

$$C_o \geq \frac{2 \cdot P_o \cdot t_{hold}}{{V_o}^2 - {V_{o.min}}^2} \geq \frac{2 \cdot 400 \cdot 16.6 \cdot 10^{-3}}{390^2 - 350^2} = 540.5\ \mu\text{F} \quad (19)$$

$$C_o \geq \frac{P_o}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_o \cdot V_o} \geq \frac{400}{2 \cdot \pi \cdot 60 \cdot 10 \cdot 390} = 272.1\ \mu\text{F} \quad (20)$$

$\rightarrow\ C_o = \max\ (272.1\ \mu\text{F}, 540.5\ \mu\text{F}) = 540.5\ \mu\text{F}$

The capacitor RMS current across the 60Hz line cycle can be calculated by the following equation, consequently the capacitor ESR loss is obtained.

$$I_{Co.rms} = \sqrt{\frac{8 \cdot \sqrt{2} \cdot {P_o}^2}{3 \cdot \pi \cdot V_{ac.min} \cdot V_o} - \frac{{P_o}^2}{{V_o}^2}} = \sqrt{\frac{8 \cdot \sqrt{2} \cdot 400^2}{3 \cdot \pi \cdot 85 \cdot 390} - \frac{400^2}{390^2}} = 2.2\ A \quad (21)$$

$$P_{Co} = {I_{Co.rms}}^2 \cdot ESR = 2.2^2 \cdot ESR = 4.84 \cdot ESR \quad W \quad (22)$$

Recommendation: 2 parallel EET-UQ2S331KF

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Heatsink

The MOSFET and diode can have separate heatsinks or share the same one, however, the selection of the heatsink is based on its required thermal resistivity.

In case of separate heatsinks for the diode and MOSFET, thermal resistors are modeled as in Figure 4.5.

$$R_{thSA.FET} = \frac{T_{J.FET} - T_A}{P_{FET}} - R_{thCS.FET} - R_{thJC.FET}$$

$$R_{thSA.diode} = \frac{T_{J.FET} - T_A}{P_{diode}} - R_{thCS.diode} - R_{thJC.diode}$$

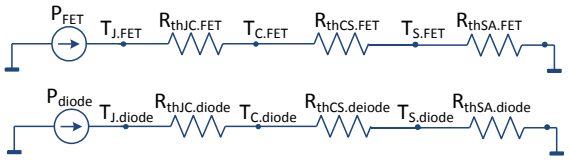

Figure 4.5

In case of a single heatsink for both the diode and the MOSFET, thermal resistors are modeled as in Figure 4.6.

The maximum heatsink temperature T_S is the minimum outcome of the two equations below

$$T_S = T_{J.diode} - P_{diode} \cdot (R_{thCS.diode} + R_{thJC.diode})$$

$$T_S = T_{J.FET} - P_{FET} \cdot (R_{thCS.FET} + R_{thJC.FET})$$

Once T_S is specified, then the heatsink thermal resistance can be calculated.

$$R_{thSA} = \frac{T_S - T_A}{P_{FET} + P_{diode}}$$

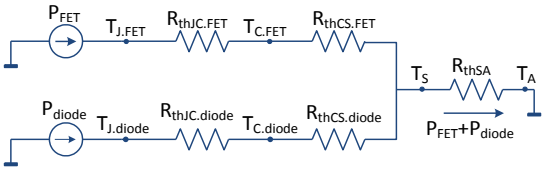

Figure 4.6

R_{thJC} is the thermal resistance from junction to case, this is specified in the MOSFET and Diode datasheets.

R_{thCS} is the thermal resistace from case to heatsink, typically low compared to the overall thermal resistance, its value depends on the the interface material, for example, thermal grease and thermal pad.

R_{thSA} is the thermal resistance from heatsink to ambient, this is specified in the heatsink datasheets, it depends on the heatsink size and design, and is a function of the surroundings, for example, a heatsink could have difference values for R_{thSA} for different airflow conditions.

T_S is the heatsink temperature, T_C is the case temperature , T_A is the ambient temperature.

P_{FET} is FET's total power loss , P_{diode} is diode's total power loss.

CCM PFC Boost Converter Design

Table 2 shows three design examples for the CCM PFC boost converter, for different power levels and switching frequencies.

Table 2

	Design Example #1	**Design Example #2**	**Design Example #3**
	400W 100kHz	**700W 80kHz**	**1000W 60kHz**
Filter Inductor			
L	416.5 µH	297.5 µH	277.7 µH
$I_{L.pk}$	7.7 A	13.4 A	19.1 A
$P_{L.cond}$	22.1 $\cdot DCR$ W	67.8 $\cdot DCR$ W	138.4 $\cdot DCR$ W
Recommendation	PFC-02301-00	PFC-05301-00	PFC-05301-00
Rectifier Bridge	GBJ1006-BP	GBJ1506-BP	GBJ2006-F
P_{bridge}	$8.3 \cdot V_{f.bridge}$ W	$14.8 \cdot V_{f.bridge}$ W	$21.2 \cdot V_{f.bridge}$ W
Recommendation	GBJ1006-BP	GBJ1506-BP	GBJ2006-F
MOSFET	IPW60R125CP	IPW60R075CP	IPW60R045CP
$I_{S.rms}$	4.04 A	7.1 A	10.1 A
$P_{S.cond}$	3.3 W	6.3 W	7.2 W
$I_{L.avg}$	4.2 A	7.4 A	10.6 A
t_{on}	$9.5 \cdot 10^{-9}$ s	$15.9 \cdot 10^{-9}$ s	$27 \cdot 10^{-9}$ s
$P_{S.on}$	0.79 W	1.8 W	3.3 W
t_{off}	$14.4 \cdot 10^{-9}$ s	$24 \cdot 10^{-9}$ s	$40.8 \cdot 10^{-9}$ s
$P_{S.off}$	1.19 W	2.8 W	5.1 W
$P_{S.oss}$	1 W	1.4 W	1.7 W
$P_{S.gate}$	0.064 W	0.084 W	0.108 W
Boost Diode	IDH12G65C5	IDW20G65C5	IDW30G65C5
$I_{D.avg}$	1.03 A	1.8 A	2.6 A
$P_{D.cond}$	1.5 W	2.7 W	3.8 W
$P_{D.sw}$	0.35 W	0.45 W	0.49 W
Output Capacitor			
C_o	540.5 µF	945.9 µF	1351 µF
$I_{Co.rms}$	2.2 A	3.8 A	5.4 A
P_{Co}	$4.84 \cdot ESR$ W	$14.5 \cdot ESR$ W	$29.6 \cdot ESR$ W
Recommendation	2 x EET-UQ2S331KF	3 x EET-UQ2S331KF	3 x EET-UQ2S331KF + 1 x EETUQ2S391LA

5 References

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CCM PFC Boost Converter Design

Symbols used in formulas

$V_{ac.min}$: Minimum input voltage
V_o: Output voltage
$V_{ac.min}$: Minimum input voltage
V_o: Output voltage
P_o: Output power
f: Switching frequency
T: Switching time period
f_{line}: line frequency
L: Filter inductor
%Ripple: Inductor current ripple percentage to input current
DCR: Inductor DC resistance
$I_{L.avg}$: Inductor average current across the line cycle
$I_{L.pk}$: Inductor peak current
$P_{L.cond}$: Inductor conduction loss
$V_{F.bridge}$: Bridge diode forward voltage drop
P_{bridge}: Bridge power loss
$R_{on(100C)}$: MOSFET on resistance at 100^{o}C
Q_{gs}: MOSFET gate-source charge
Q_{gd}: MOSFET gate-drain charge
Q_g: MOSFET total gate charge
R_g: MOSFET gate resistance
V_{pl}: MOSFET gate plateau voltage
V_{th}: MOSFET gate threshold voltage
t_{on}: MOSFET switching on time
t_{off}: MOSFET switching off time
E_{oss}: MOSFET output capacitance switching energy
$I_{S.rms}$: MOSFET rms current across the line cycle
$P_{S.cond}$: MOSFET conduction loss
$P_{S.on}$: MOSFET switching on power loss
$P_{S.off}$: MOSFET switching off power loss
$P_{S.oss}$: MOSFET output capacitance switching loss
$P_{S.gate}$: MOSFET gate drive loss
$I_{D.avg}$: Boost diode average current
$V_{F.diode}$: Boost diode forward voltage drop
Q_{rr}: Boost diode reverse recovery charge
P_{Dcond}: Boost diode conduction loss
$P_{D.sw}$: Boost diode switching loss
C_o: Output capacitor
ESR: Output capacitor resistance
t_{hold}: Hold-up time
$V_{o.min}$: Hold up minimum output voltage
ΔV_o: Output voltage ripple
$I_{Co.rms}$: Output capacitor rms current
P_{Co}: Output capacitor conduction loss