



## UNIVERSAL OUTPUT

LVPECL LVDS  
LVCMOS HCSL

### FEATURES

- Up to two / four high-performance universal outputs
  - Each configurable as one differential output pair or two LVCMOS outputs
  - Low RMS additive phase jitter: 0.2 ps
- One additional LVCMOS clock output
- I/O standards:
  - Single-ended I/Os: 1.8 V to 3.3 V LVCMOS
  - Differential I/Os - LVPECL, LVDS and HCSL
- Input frequency ranges:
  - LVCMOS reference clock input 1 MHz to 200 MHz
  - LVDS, LVPECL, HCSL differential clock input (CLKIN,CLKINB) – 1 MHz to 350 MHz
  - Crystal frequency range: 8 MHz to 40 MHz
- Four banks of internal non-volatile in-system programmable or factory-programmable OTP memory
- I<sup>2</sup>C serial programming interface
- Individually selectable input and output voltage (1.8 V, 2.5 V, 3.3 V) for each output pair
- 4 x 4 mm VQFPN 24-pin package

## Flexible, low-jitter universal output buffers

The 5P1103 and 5P1105 are programmable universal fanout buffers with universal outputs intended for high-performance consumer, networking, industrial, computing, and data communications applications. Configurations can be stored in on-chip one-time programmable (OTP) memory or changed using an I<sup>2</sup>C interface. The memory in the devices can be programmed or ordered with factory programmed specifications.

The universal outputs allow engineers to use one device to meet the requirements of systems featuring multiple signal types. Users can specify the signal type and voltage of each output on the buffer. For example, a single device can supply LVPECL on one output, LVDS on another, and LVCMOS on a third. The flexibility and low jitter make these buffers ideal for timing SoCs and FPGAs. The small package and flexible output configuration saves board space, reduces component count and lowers system cost.

To learn more about IDT's Programmable Universal Output Buffers, visit: [IDT.com/5P1103](http://IDT.com/5P1103) | [IDT.com/5P1105](http://IDT.com/5P1105)